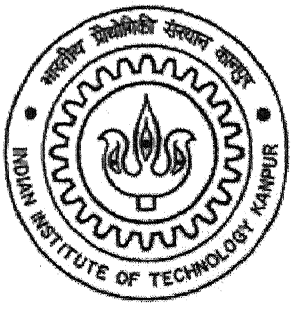
DESIGN OF A THIRD ORDER CASCADED (2-1) SIGMA–DELTA MODULATOR

A Thesis Submitted
In Partial Fulfillment of the Requirements
For the Degree of

Master of Technology

by

Praveen Madhunapantula



to the
Department of Electrical Engineering
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Under the Supervision of

Dr. Animesh Biswas

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CERTIFICATE

This is to certify that the work contained in this M.Tech thesis entitled "**Design of a Third Order Cascaded (2-1) Sigma–Delta Modulator**", by Mr. Praveen Madhunapantula (Roll No. Y3104064) has been done under my supervision. This work has not been submitted elsewhere for a degree.

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Dedicated

to

Mum, Dad & Brother

ACKNOWLEDGEMENTS

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Next, I would like to acknowledge my family, especially my brother. Although far away, thoughts of them pervade my mind everyday. Strength and equanimity springs from knowledge of their well being and health. I hope and wish for their reciprocating happiness always.

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Finally, I would like to express my gratitude to the God, for this beautiful life he has given to me. I must say, "Lucky is my life".

Praveen Madhunapantula

ABSTRACT

The use of oversampling sigma-delta (ΣΔ) modulators in the integration of high-resolution analog-to-digital converters has shown promise for overcoming the analog component limitations inherent in modern VLSI technologies. The design of a switched-capacitor (SC) ΣΔ modulator with third order (2-1) cascaded (MASH) architecture for 320 KHz baseband bandwidth is presented in this work. A behavioral model for a SC ΣΔ modulator is presented, where most of its nonidealities are considered and performed the time domain behavioral simulations. A low power, fully differential operational transconductance amplifier (OTA) is used in the transistor level design. The transistor level SC ΣΔ modulator is implemented using 0.25μm CMOS technology with a single 3V power supply. For a 50 KHz input signal, the modulator achieves a signal-to-noise ratio (SNR) of 83 dB with an oversampling rate of 64.

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Chapter 1

INTRODUCTION

1.1 BACKGROUND

With the continued scaling of integrated circuit technologies and digital storage media, digital signal processing systems have supplanted their analog counter parts in many applications. Since digitally processed signals usually originate in the analog domain and once processed must be returned to the analog domain, the proliferation of digital processing systems has generated the need for high–performance analog–to–digital (A/D) and digital–to–analog (D/A) converters. Many factors including cost, reliability, size and speed, have fueled the desire to implement these converters in the same integrated circuit technologies that provide the inexpensive high–speed medium for digital processor design. However the precision with which components match in scaled integrated circuit technologies is often less than the desired converter precision and thereby limits the accuracy that can be achieved in A/D and D/A converters.

The use of oversampling sigma–delta (ΣΔ) modulators in the integration of high–resolution analog–to–digital converters has shown promise for overcoming the analog component limitations inherent in modern VLSI technologies. Oversampling analog–to–digital converters based on the ΣΔ modulation offer high–precision conversion with out the requirements of excessive component matching at the expense of speed. This speed penalty becomes less severe when a higher order noise shaping is realized. Sigma–delta modulators employ coarse quantization enclosed in one or more feedback loops. By sampling at a frequency that is much greater than the signal bandwidth, it is possible for the feedback loops to shape the quantization noise so that most of the noise power is shifted out of the signal band. The out of band noise can then be attenuated with a digital filter. The degree to which the quantization noise can be attenuated depends on the order of the noise shaping and the oversampling ratio.

Second order ΣΔ modulators have been successfully used for audio applications. However, since the quantization noise is only second–order shaped, an oversampling ratio of 256 that is, a sampling frequency as high as 81.92 MHz for a 160 KHz baseband, is necessary to realize 16 bit resolution. A conventional single–loop ΣΔ modulator with an order higher than two may oscillate. The loop can be made stable by proper scaling of the integration gain factors, due to the limitation effect on the internal signals by the supply voltages. However, the resulting noise shaping is much worse than the corresponding ideal one. Also, large integration capacitances are needed to realize the low gain factors, which introduce high parasitic bottom capacitances at the op–amp outputs. Multistage ΣΔ converters based on stable first or second order ΣΔ modulators give the possibility of realizing almost ideal higher order (i.e., more than second order) noise shaping. The disadvantage is that their performance is more sensitive to the nonideal components used in the modulator.

A complete ΣΔ A/D converter comprises two main components: a modulator and a decimation filter. The modulator is an analog circuit and usually limits the performance of the converter. This work concentrates on the modulator.

1.2 ORGANIZATION OF THE WORK

In this thesis, a third order 2-1 cascaded (MASH) ΣΔ modulator is described and modeled its behavior in Matlab, Simulink with considering most of its nonidealities. This is compared by the transistor level design.

Chapter 2 introduces the fundamentals of oversampled sigma–delta modulator design. System-level trade-offs including single-loop versus cascaded architectures, continuous-time versus sampled-data and single–bit versus multi–bit ΣΔ modulators are discussed here. A third order 2-1 cascaded (MASH) sigma delta modulator is briefly discussed here.

System level architecture design of the ΣΔ modulator is presented in Chapter 3. Building blocks of an ideal 2-1 cascaded ΣΔ modulator are discussed here. Later different nonidealities present in the ΣΔ modulator is described and modeled in Matlab, Simulink. A second order ΣΔ modulator is designed using the proposed Simulink model and verified.

Chapter 4 focuses the circuit implementation of the ΣΔ modulator, with an emphasis on low power optimization. Key trade-offs and challenges in the design of the transconductance amplifier, common-mode feedback network, sampling switches, biasing and digital circuits are discussed.

Behavioral simulation results of an ideal and nonideal model of a third order 2-1 cascaded ΣΔ modulator are presented in Chapter 5. The transistor level simulation results are also described. Behavioral level simulations are done using Matlab, Simulink. Transistor level simulations are done using Tanner tools and Matlab.

Conclusions from this work are given in Chapter 6.

Chapter 2

REVIEW OF SIGMA-DELTA (ΣΔ) MODULATORS

2.1 INTRODUCTION

Modern electronics systems make extensive use of digital signal processing, but require analog-to-digital (A/D) and digital-to-analog (D/A) converters to interface to the real analog world. Sigma Delta (ΣΔ) modulators trade resolution in time for resolution in amplitude such that the use of imprecise analog circuits can be tolerated. Sigma-Delta Analog-Digital Converters (ΣΔADC) have been known for nearly forty years, but only recently has the technology (high-density digital VLSI) existed to manufacture them as inexpensive monolithic integrated circuits. They are now used in many applications where a low-cost, low-bandwidth, low-power, high-resolution ADC is required [1][2][7][10][11].

This chapter reviews some of the fundamental issues of analog-to-digital conversion and ΣΔ modulation. The chapter begins with a discussion of the quantization noise of Nyquist rate converters and ΣΔ converters are made. Next section addresses various ΣΔ choices with an emphasis on topologies. A

comparison of discrete and continuous time ΣΔ modulators are discussed in the next section. Brief discussions on the metrics that are used to evaluate the performance of ΣΔ modulator are given. In the next section, different cascaded topologies used for ΣΔ modulators are discussed. Finally brief comparisons of single bit and multi-bit ΣΔ modulators are discussed.

2.2 QUANTIZATION NOISE

2.2.1 NYQUIST RATE CONVERTERS

Quantization of amplitude refers to the "mapping" of a continuous amplitude signal to a finite number of discrete levels, is at the heart of all digital modulators. The difference between the original continuous amplitude and the new "mapped" value represents the quantization error. Figure 2.1 illustrates the quantization process. Qualitatively, it can be observed that the quantization error gets smaller as the number of discrete levels increases. The number of levels is in turn proportional to the resolution of the quantizer used in the ADC. Increasing the quantizer resolution will decrease the quantization error [2][14][15].

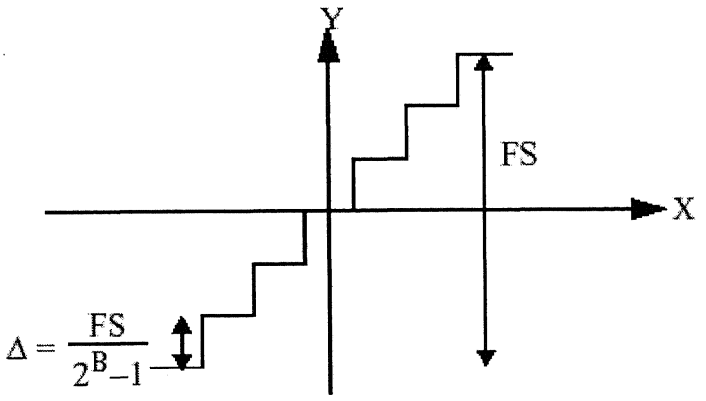


FIGURE 2.1 QUANTIZATION PROCESS

The error is a strong function of the input; however, if the input changes randomly between samples by amounts comparable to or greater than the spacing of the levels, then the error is largely uncorrelated from sample to sample and has equal probability of lying anywhere in the range of ± Δ/2 [1]. Further, if it is assumed that the error has statistical properties which are independent of the signal, the error can then be represented by a noise.

The quantization noise is given by the mean-square value of the quantization error described above. Using a double-sided spectrum, the quantization noise is given by

$$P_{Q,Nyquist} = \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} q^2 dq = \frac{\Delta^2}{12} \tag{2.1}$$

and is assumed to fall between $-fs/2$ and $+fs/2$, where fs is the sampling frequency. In Nyquist rate converters, the sampling frequency is usually twice the signal bandwidth i.e.

$$f_S = 2f_{BW} \tag{2.2}$$

where f_{BW} is the signal bandwidth.

2.2.2 OVERSAMPLED CONVERTERS

Oversampled converters run at sampling frequencies greater than twice the signal bandwidth. From Eq (2.1), the quantization noise power is independent of the sampling rate. As such, the quantization noise power in oversampled converters is the same as that for Nyquist-rate converters, but is now distributed over a wider band, as shown in Figure 2.2 [2][15]. The in-band quantization noise is shown by the shaded region, and is given by

$$P_{Oversampled} = \int_{-f_{BW}}^{f_{BW}} \frac{\Delta^2}{12}\frac{1}{f_S} df = \frac{P_{Q,Nyquist}}{f_s/2f_{BW}} = \frac{P_{Q,Nyquist}}{M} \tag{2.3}$$

where M is oversampling ratio given by

$$M = f_S/2f_{BW} \tag{2.4}$$

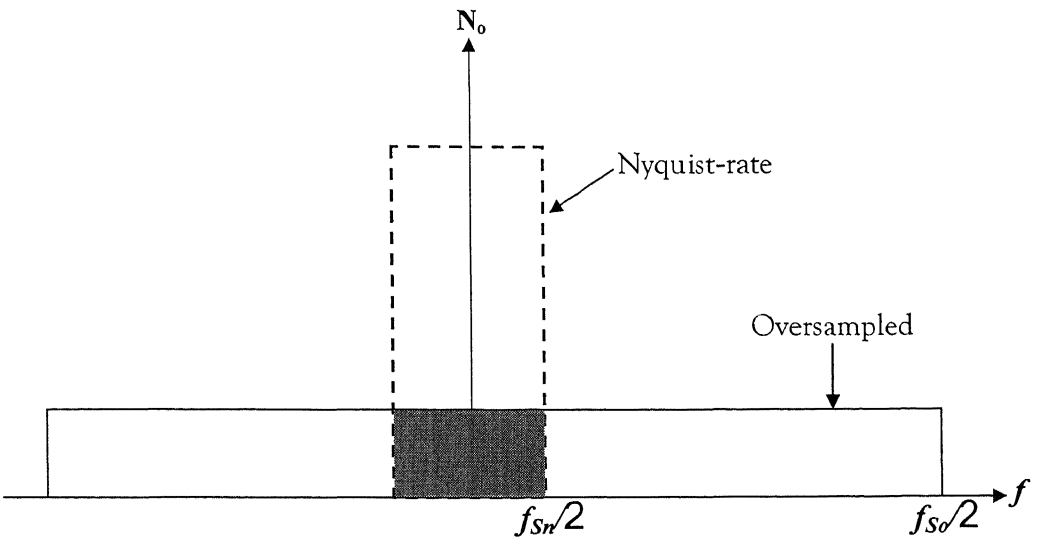


FIGURE 2.2 QUANTIZATION NOISE SPECTRUM IN NYQUIST-RATE AND OVERSAMPLED CONVERTERS

Increasing the sampling rate therefore reduces the quantization noise power by a fraction M, which is equal to the oversampling ratio. In the above figure f_{So} and f_{Sn} represents the sampling frequency of Oversampled and Nyquist rate converters. The above analysis assumes that the quantization noise spectrum is white; however, this is not the case in practical systems. A complete modeling of the quantization noise as an additive white-noise source was performed in [15].

2.2.3 Sigma-Delta Converters

Sigma-delta modulator employs negative feedback in addition to oversampling to further reduce the in-band quantization noise. Figure 2.3 (a) shows a basic first-order sigma delta modulator. Due to the negative feedback, the output Y will, on average, be force to equal the input signal X. By oversampling the input and then averaging the output, we can very accurately predict the input signal without the need for a high resolution quantizer.

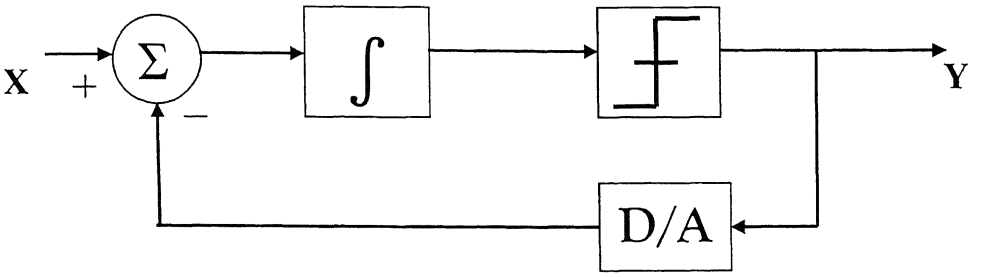


FIGURE 2.3(a) SIMPLIFIED BLOCK DIAGRAM

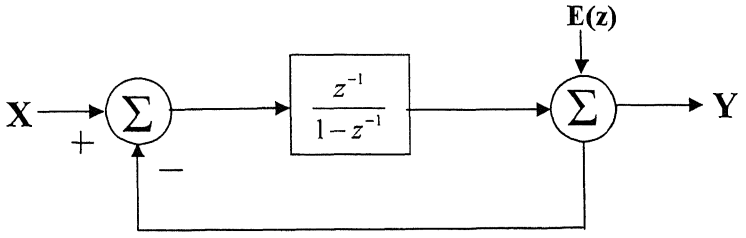


FIGURE 2.3(b) LINEARIZED MODEL

FIGURE 2.3 FIRST ORDER SIGMA DELTA MODULATOR

The first-order sigma-delta modulator can be represented by the linearized model shown in Figure 2.3 (b). There are two important transfer functions that can be determined from Figure 2.3(b): the signal transfer function (STF) and the noise transfer function (NTF). Using simple feedback analysis, they are given by

$$STF = \frac{Y(z)}{X(z)} = \frac{\frac{z^{-1}}{1-z^{-1}}}{1+\frac{z^{-1}}{1-z^{-1}}} = z^{-1} \tag{2.5}$$

$$NTF = \frac{Y(z)}{E(z)} = \frac{1}{1+\frac{z^{-1}}{1-z^{-1}}} = 1-z^{-1} \tag{2.6}$$

Therefore, the STF is simply a unit delay. A signal that is input to the ΣΔ is passed through without any frequency distortion. The NTF, however, has a frequency-selective characteristic, shaping the additive white noise source, $E(z)$, with a high pass characteristic [1][15].

Since the transfer function from the quantization error source to the output is given by $(1-z^{-1})$ the noise is shaped by a high-pass characteristic. This suppresses the in-band noise, as quantified by

$$P_{Q,\Sigma\Delta} = \int_{f_{BW}}^{f_{BW}} \frac{P_{Q,Nyquist}}{M}(1-z^{-1})df \approx \frac{P_{Q,Nyquist}}{M^3}\frac{\pi^2}{3} \qquad (2.7)$$

for M >>1

The feedback loop at the heart of sigma-delta modulators is clearly a noise-shaping filter which attempts to cancel the in-band quantization noise by predicting the value of the noise. Higher-order modulators can better predict (and therefore cancel) the in-band quantization noise. A simple feedback theory analysis will show that the transfer function from the quantization noise source to the output is given by $(1-z^{-1})L$, where L is the order of the sigma-delta modulator. This is given by the equation below.

$$P_{Q,\Sigma\Delta} = \int_{f_{BW}}^{f_{BW}} \frac{P_{Q,Nyquist}}{M}(1-z^{-1})^L df \approx \frac{P_{Q,Nyquist}}{M^{2L+1}}\frac{\pi^{2L}}{2L+1} \qquad (2.8)$$

for M >>1

Below is a generalized equation for the in-band quantization in a L-order sigma-delta modulator. The dynamic range (with quantization noise being the only noise source) can be easily derived and is shown below.

$$DR_{\Sigma\Delta} = 10\log\left[\frac{3}{2}(2^B-1)^2\frac{2L+1}{\pi^{2L}}M^{2L+1}\right]^{2L+1} \qquad (2.9)$$

where L is the order of modulator
M is the oversampling ratio
B is the resolution of quantizer

It can be observed that the dynamic range can be increased by increasing the modulator order, the oversampling ratio, or the quantizer resolution. For every doubling of the oversampling ratio, the dynamic range increases by 3(2L+1) dB or (L+0.5) bits.

The disadvantage of using higher-order modulators (3rd-order or higher) is that the modulators may experience limit-cycle oscillations or instability. Techniques to overcome this problem are discussed in [1].

2.3 LOOP FILTER TOPOLOGIES

This section aims to review the fundamentals of sigma-delta loop filter design; the topologies presented here are not intended to be an exhaustive in nature; rather, they only represent a cross-section of common commercially-implemented filter designs today. The modulator order is determined by the number of integrator stages in the forward path. In each of the filter topology below, the transfer function from the quantization-noise source to the output will be presented [1][10].

Figure 2.4 illustrates the distributed feedback filter topology for a 4th-order modulator. The output Y(z) is fed back to each of the four integrators through gain stages, a_1-a_4. The quantization noise transfer function, $H_e(z)$, to the output is given by

$$H_e(z) = \frac{(z-1)^4}{(z-1)^4 + a_4(z-1)^3 + a_3(z-1)^2 + a_2(z-1) + a_1} \tag{2.10}$$

Note that all the zeros are at z = 1. In the frequency domain, this means the zeros are all at DC. The poles can be implemented using a Butterworth high-pass response for a maximally flat quantization noise spectrum at high frequency.

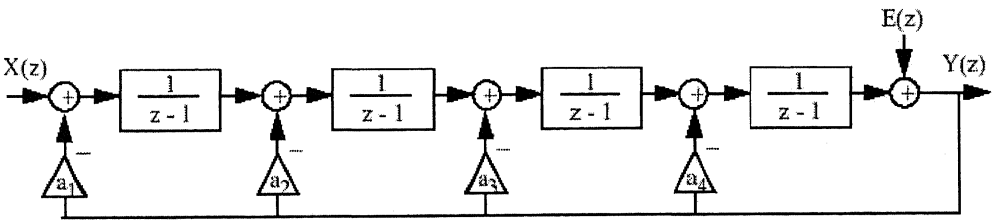


FIGURE 2.4 DISTRIBUTED FEEDBACK TOPOLOGY

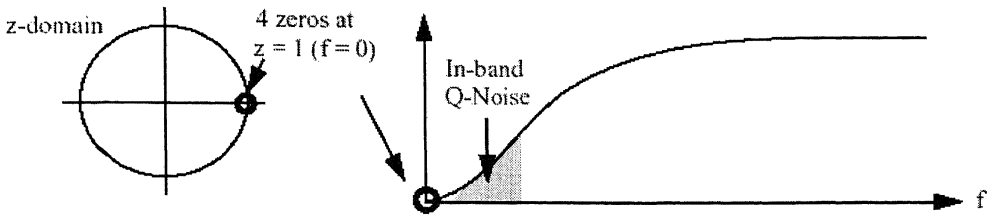


FIGURE 2.5 FREQUENCY RESPONSE OF FEEDBACK, FEEDFORWARD SUMMATION TOPOLOGIES

An "inverted" form to the previous topology is shown in Figure 2.6. The output of each integrator is gained and then summed together before feeding into the quantizer. It can be easily shown that the quantization noise transfer function is identical to that for the Distributed Feedback structure, and is given by Eq. (2.8).

An effective way of suppressing the in–band quantization noise is to spread the zeros over the signal bandwidth instead of placing them all at DC. This can be accomplished by adding local resonator feedback loops in either the distributed feedback or feedforward summation topologies. The resonators create

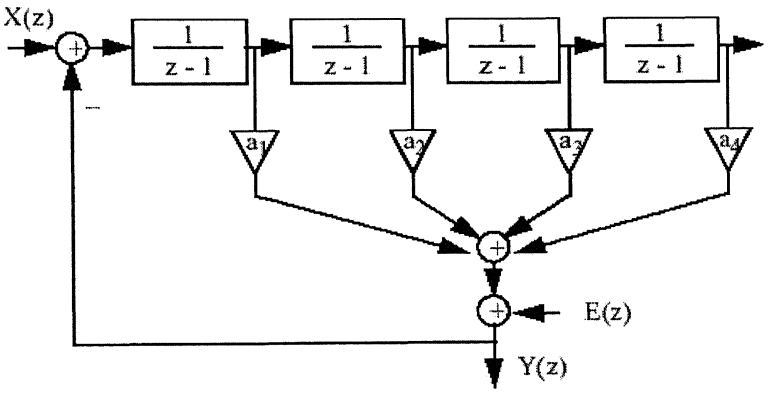


FIGURE 2.8 FEEDFORWARD SUMMATION TOPOLOGY

pairs of complex zeros which will allow the use of an Inverse Chebychev response. The distributed feedback topology using local resonators is shown in Figure 2.9 and its frequency response is shown in Figure 2.10.

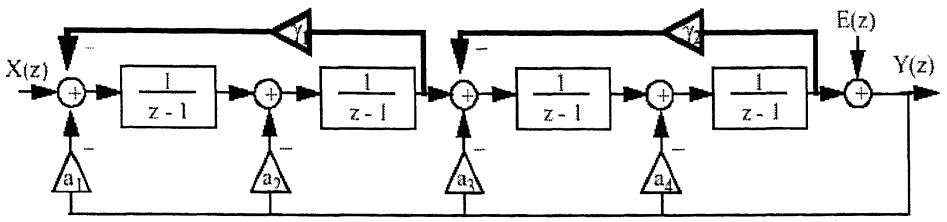


FIGURE 2.9 DISTRIBUTED FEEDBACK WITH LOCAL RESONATOR FEEDBACK TOPOLOGY

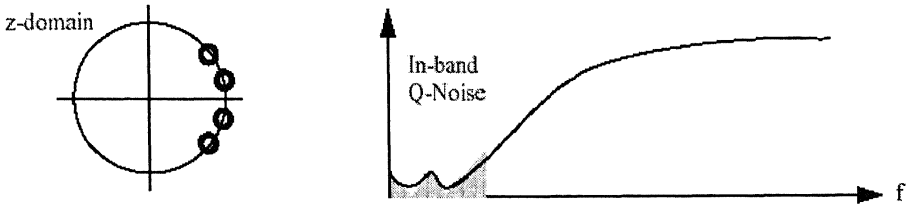


FIGURE 2.10 FREQUENCY RESPONSE FOR DISTRIBUTED FEEDBACK TOPOLOGY USING LOCAL RESONATORS FEEDBACK

2.4 SAMPLED-DATA VS. CONTINUOUS-TIME

Sigma-delta modulators can be implemented either as a sampled-data system or in the continuous-time domain. The primary difference is that sampled-data sigma-delta systems employ switched-capacitor integrators while continuous-time systems use active-RC integrators in the modulators. There are a number of advantages and disadvantages associated with each option, as will be discussed below [1][8][[14].

Switched-capacitor integrators take advantage of fine-line VLSI capabilities by eliminating the need for physical resistors. On-chip resistors with very high linearity are difficult to achieve in standard CMOS process. In addition, resistors in continuous-time integrators need to be kept small to minimize thermal noise. For the same time-constant, reducing the resistors implies that the feedback capacitors need to be increased. This may make the area prohibitively large and the capacitors impractical to realize on-chip.

The frequency response of switched-capacitor integrators can be more accurately predicted because the time-constant is a function of capacitor ratios

(C_S/C_I) and of the sampling frequency [28]. The time-constant of continuous-time integrators, on the other hand, is a product of the resistor and the capacitor, and suffers severely from process variations. The absolute value of on-chip poly resistors typically vary by 30% from the nominal/desired value, whereas capacitor ratios are usually better controlled (typical variation is only 1%).

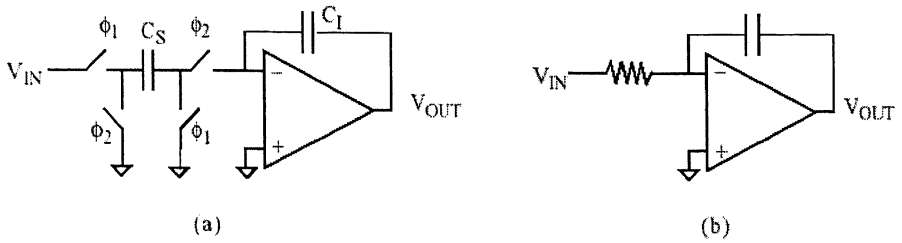


FIGURE 2.11: (a) SWITCHED CAPACITOR INTEGRATOR (b) CONTINUOUS TIME INTEGRATOR

Another advantage of switched-capacitor sigma-delta systems is that they are less sensitive to clock jitter and to the manner in which the opamp settles [1]. As long as the opamp settles to the required accuracy, it does not matter whether the opamp slews or linearly settles. Continuous-time integrators, however, must be linear at all times.

Continuous-time systems have their share of advantages over sampled-data systems. Because the opamp in an active-RC integrator does not have to settle to full accuracy every half clock period, a very high oversampling ratio is achievable [1]. The oversampling ratio in switched-capacitor integrators is limited by the achievable bandwidths of the opamps. This makes continuous-time sigma-delta modulators very appealing for high-speed applications.

Finally, continuous-time systems eliminate the need for an anti-alias filter prior to the sigma-delta ADC. The anti-alias filter is needed in sampled-data systems to attenuate energies at multiples of the sampling frequency which may potentially fold down to baseband. The elimination of this filter results in significant power savings for the receiver.

2.5 PERFORMANCE METRICS

This section defines the metrics used to evaluate ΣΔ modulator performance. The key requirements for a ΣΔ modulator are dynamic range, Nyquist rate, peak signal to noise ratio (SNR), peak signal to noise and distortion ratio (SNDR), which measure the degradation of the signal due to noise alone, and due to combination of noise and distortion respectively [1][17][15].

2.5.1 PEAK SNR/SNDR AND DYNAMIC RANGE

Peak SNR, SNDR and dynamic range are related specifications and will be defined together. Dynamic range is the ratio in power between the maximum input signal level that the modulator can handle and the minimum detectable input signal. SNR is the ratio of the signal power at the output of the modulator to the noise power. SNR includes all noise sources in the modulator, both thermal and quantization. SNDR is the ratio of the signal power at the output of the modulator to the sum of the noise and harmonic distortion powers. Peak SNDR is a useful metric for evaluating the capability of a sigma-delta modulator for handing large in band signals at acceptable linearity and is especially important for applications such as digital audio. Note that peak SNDR is frequency dependent and can be used to measure the degradation of modulator performance as the input signal increases in frequency.

Peak SNR, SNDR and dynamic range are typically reported using the type of plot shown in Fig. 2.12. The plot shows SNR and SNDR as a function of input signal power in dB relative to the full scale of the modulator. For small signal levels, distortion is not important implying that the SNR and SNDR are approximately equal. As the signal level increases, distortion degrades the modulator performance, and the SNDR will be less than the SNR. Dynamic range on the plot is the difference between the input level where the SNDR drops 3 dB beyond the peak and the x-intercept of the SNDR curve.

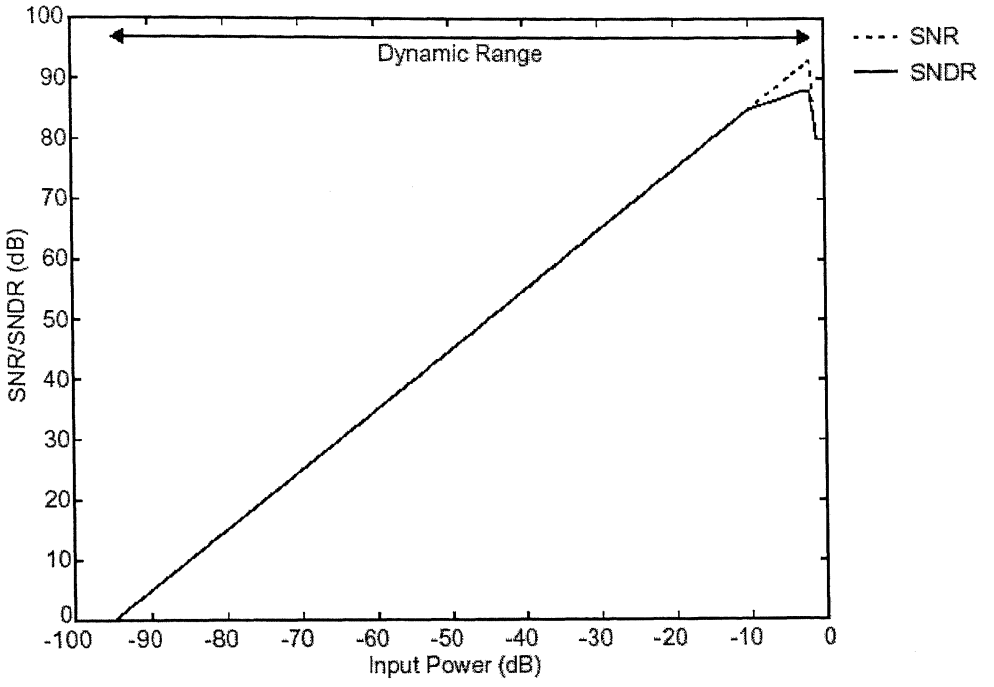


FIGURE 2.12 SNR AND SNDR CURVES

2.5.2 EFFECTIVE NUMBER OF BITS

A closely related specification to dynamic range is the resolution of the modulator expressed in bits. Effective number of bits (N) gives an indication of how many bits would be required in an ideal quantizer to get the same performance as the converter. This number also includes the distortion components and can be calculated as

$$N = \frac{SNDR_p - 1.76}{6.02} \tag{2.11}$$

2.5.3 NYQUIST RATE

The Nyquist rate is a measure of the speed of a sigma-delta modulator. The Nyquist sampling theorem states that to avoid aliasing, a low-pass signal must be sampled at a rate that is twice its bandwidth. As a result, specifying the Nyquist rate is equivalent to specifying the modulator input bandwidth.

2.6 CASCADED TOPOLOGIES

By increasing the order of the ΣΔ modulators, results in stability problems and a reduction of the overload level. For single bit converters, the stability problem requires small coefficients resulting in a severe degradation of peak SNR compared to an ideal n^{th} order ΣΔ modulator. This effect significantly limits the benefits of increasing the order of the ΣΔ modulators.

This problem can be overcome by employing cascaded topologies. This will allow the combination of a high order noise shaping with the intrinsic stability of a 2^{nd} order ΣΔ modulator. The cascaded ΣΔ modulator consists of several stages of low-order ΣΔ modulators. Each stage converts the quantization error of the previous stage. By combining the digital outputs of all the stages with the proper transfer function in the digital domain, the quantization errors of all stages but the last one can be canceled. The only quantization error that remains visible at the output is the quantization noise of the last stage, which is shaped by the total number of integrator in the cascaded ΣΔ modulators [2][3].

Any single loop ΣΔ modulator can be used as a stage of a cascaded ΣΔ modulator. Only first and second order single loop ΣΔ modulators are used, because they are more stable. One of the main advantages of a cascaded ΣΔ modulator is that it can achieve high-order noise shaping while maintaining intrinsic stability. Therefore, third and higher order singe loop ΣΔ modulators are not used since they are not unconditionally stable.

First order modulator is not used as a first stage of cascaded ΣΔ implementation because the output of a first order single loop modulator contains a lot of in-band tones. This is due to the fact that the input of the quantizer is not random, and results in a highly colored quantization error. However, a first order ΣΔ loop can be used in subsequent stages of a cascaded modulator. Since the input of the first order stage now consists of the quantization error of the previous stage, the input of the quantizer of the first order loop will be randomized enough to get rid of the tones in the output spectrum. Hence most cascaded ΣΔ implementation

uses second order ΣΔ loop as its first stage. The performance of a cascaded modulator is more sensitive to imperfections of the analog components than that of the single loop modulator.

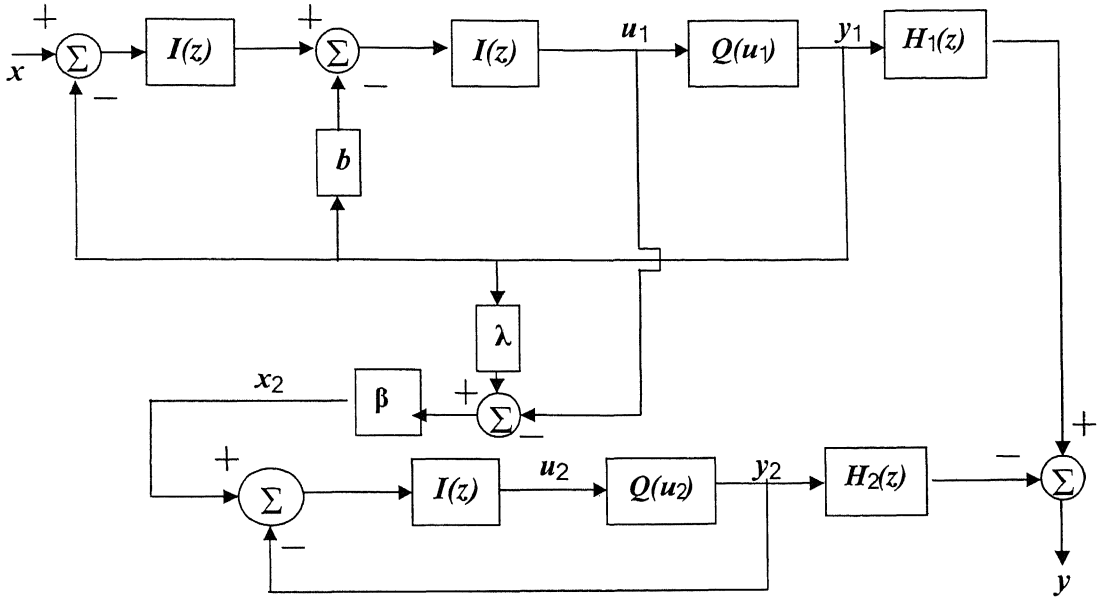


FIGURE 2.13 THE 2-1 CASCADED MASH ARCHITECTURE

A block diagram of the 2-1 cascaded MASH ΣΔ architecture is shown in Figure 2.13. It is a cascade of a second-order modulator followed by a first order modulator coupled through an error mixing network formed by β and λ. The quantized output of which modulator is combined in a digital filtering network designed to cancel the quantizer error of the first stage.

In this figure, $I(z)$ represents the z transform of a delaying integrator, which ideally is

$$I(z)=\frac{z^{-1}}{1-z^{-1}} \tag{2.12}$$

and $Q(u)$ represents a one-bit, or two-level quantization and is defined as

$$Q(u)=\begin{cases}\frac{1}{2}, & u\geq 0\\ -\frac{1}{2}, & u<0\end{cases} \tag{2.13}$$

The value of b affects both the overload level of the modulator and the location and amplitude of spectral noise tones in the output [4]. The value of coefficient b is chosen to be 2.5. Each quantizer can be modeled as an effective linear gain plus an additive error term.

$$Q(u_k) = G_k u_k - e_k \tag{2.14}$$

where k is 1 for first stage and 2 for second stage. If D/A errors are neglected and it is assumed either that the quantizer has a linear gain term of unity i.e, G_1 and G_2 are equal to 1. The modulator outputs are :

$$Y_1(z) = z^{-2}X(z) + (1-z^{-1})^2 E_1(z) \tag{2.15}$$

$$Y_2(z) = z^{-1}X_2(z) + (1-z^{-1})E_2(z) \tag{2.16}$$

where $E_1(z)$ and $E_2(z)$ are the z-transforms of the quantizer errors for the first and second stages respectively. The input to the second stage is

$$X_2(z) = \beta[(\lambda-1)Y_1(z) + E_1(z)] \tag{2.17}$$

where λ is the error mixing coefficient and β is the error gain coefficient. The overall output of the 2–1 architecture, Y(z), is given by

$$Y(z) = H_1(z)Y_1(z) - H_2(z)Y_2(z) \tag{2.18}$$

The digital filters $H_1(z)$ and $H_2(z)$ are chosen such that the quantizer error of the first stage, $E_1(z)$, is canceled. The transfer function of $H_1(z)$ and $H_2(z)$ is given by

$$H_1(z) = z^{-1} - a(1-z^{-1})z^{-1} \tag{2.19}$$

$$H_2(z) = \frac{1}{\beta}(1-z^{-1})^2 \tag{2.20}$$

If higher order difference terms are neglected, it follows from equations (2.12) - (2.20), that the overall output Y(z) is

$$Y(z) \approx z^{-3}X(z) + (1-z^{-1})^3 \left[(a+1-b+\frac{1}{G_2})\frac{E_1(z)}{G_1} - \frac{1}{\beta}\frac{E_2(z)}{G_2} \right] \tag{2.21}$$

where X(z) is the z transform of the modulator input, $E_1(z)$ and $E_2(z)$ are the z transforms of the quantizer errors, G_1 and G_2 are the effective gains of the quantizers and a is chosen to cancel the first stage error term. Delays and higher order terms are neglected.

From equation (2.21) it is apparent that $E_2(z)$, is shaped by a third order difference similar to that of a third order single stage sigma delta modulator. With matching errors, some of the first stage error, $E_1(z)$, appears at the output, and that error is shaped by a second order difference. For different values of b,β and λ, there is a tradeoff between quantization noise and the input level at which the modulator overloads. The optimized values for these parameters are taken from [5] are b = 2.5, β = 0.5 and λ = 2.0. The choice of the appropriate error cancellation parameter a in equation (2.19) requires an estimate of the effective quantizer gain. Here we assumed that the value of a is 0.517 from [5].

2.7 SINGLE-BIT VS MULTI-BIT

ΣΔ modulators employ single-bit quantizer or multi-bit quantizer. Single bit quantizer has only two levels where as multi-bit quantizer have multiple levels. Multi-bit ΣΔ modulators have better performance when compare to the single-bit ΣΔ modulators. This is due to the decrease of the step size of the quantizer, which leads to a lower quantization error. However, due to the stabilizing action of the multi-bit quantizer, a more aggressive noise shaping function can be used resulting in a better suppression of the quantization noise [1][15].

The accuracy of high-order topologies only benefits in combination with a large oversampling ratio, but multi-bit quantization offers an intrinsic improvement of the accuracy for all oversampling ratios. The multi-bit single loop topologies do not suffer from noise leakage. Therefore, the building block specification will be more relaxed than for a cascaded implementation.

The main problem of multi-bit ΣΔ modulators is the linearity requirement imposed on the DAC in the feedback path. As the number of bits is increased the complexity of the implementation of the quantizer and the DAC also increases. While, a single-bit feedback DAC is inherently linear, the linearity of a multi-level is limited by component matching of its individual components, hence the complexity increases.

2.8 SUMMARY

This chapter reviewed important concepts in the design of ΣΔ modulators. The benefits of ΣΔ modulators as data converters were first presented, and were contrasted with conventional Nyquist rate converters. The concept of noise shaping of a ΣΔ modulator was discussed. Next, various options of filter design were investigated, with emphasis on strategies to suppress the in-band quantization noise by spreading the zeros over the signal bandwidth. This was followed by a discussion on sampled-data versus continuous-time implementations. Next, different metrics used to evaluate the performance of ΣΔ modulators are discussed. This was followed by a discussion on MASH or cascaded architecture. The chapter concluded with the comparison of single-bit and multi-bit ΣΔ modulators. The implications and severity of the non-idealities will be presented in the next chapter.

Chapter 3

MODULATOR DESIGN

3.1 INTRODUCTION

Transferring the block diagram of the 2-1 architecture to a device-level description involves the design of circuits that implement summing integrators, comparators, and one-bit D/A converters. Circuit deficiencies such as finite speed, thermal noise, and finite signal swing limit the performance of the modulator. A significant problem in the design of ΣΔ modulators is the estimate of their performance, since they are mixed-signal nonlinear circuits. Due to the inherent nonlinearity of the ΣΔ modulator loop the optimization of the performance has to be carried out with the behavioral time-domain simulations. This becomes difficult for a high performance system. To satisfy high performance system requirements, accurate simulations of a number of non-idealities are to be considered. In the design of high-resolution switched-capacitor (SC) ΣΔ modulators, a large set of parameters, including the performance of building blocks, are to be optimized in

order to achieve the desired performance metrics like signal-to-noise ratio (SNR) and Dynamic range [1][15].

The first section in this chapter introduces the circuit blocks that compose a noise-differencing ΣΔ modulator, and these blocks are combined to produce a 2-1 cascaded or MASH architecture. In the next section, the major non-idealities of SC ΣΔ modulators are described and the correspondent behavioral model blocks are then presented. Finally, a second-order sigma delta modulator using our proposed behavioral model is discussed and compared with the actual model presented in [12].

3.2 MODULATOR BUILDING BLOCKS

Typically the most important building blocks in the analog portion of a noise differencing sigma-delta modulator are the summing integrators. These integrator circuits are normally designed to implement the block diagram shown in Figure 3.1 [10][15].

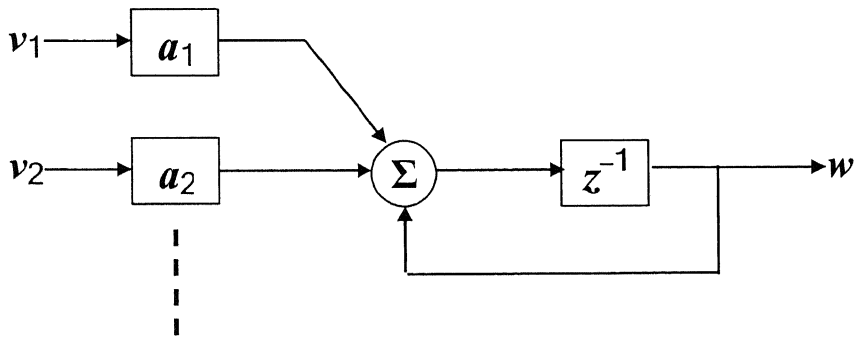


FIGURE 3.1 INTEGRATOR BLOCK DIAGRAM

The output of this integrator, w is a delayed integration of a weighted sum of inputs, v_i. In the time domain, the output is

$$w((n+1)T_S) = w(nT_S) + \sum_m a_m v_m(nT_S) \tag{3.1}$$

where T_S is the sampling period. The output can also be written in the z-transform domain as

$$W(z) = \frac{z^{-1}}{1-z^{-1}} + \sum_m a_m V_m(z) \tag{3.2}$$

where $V_i(z)$ and $W(z)$ are the z-transform of v_i and w, respectively.

The remaining building blocks in the analog portion of the modulator are comparators and one bit D/A converters. The comparator circuit's act as a one bit A/D converter, they map their inputs to two digital output codes. These two digital output codes are then mapped back into analog levels by the D/A converters. For simplicity, let the two output codes of the comparators be defined as ±1/2. With this definition, the comparators can be described by the quantization function Q(x) defined in Eq. 2.13 and the D/A converters, neglecting D/A errors, can be represented simply by gain blocks.

By combining three summing integrators with two comparators and two one bit D/A converters, 2-1 architecture can be constructed as shown in Figure 3.2. The D/A converters are represented by the gain blocks Δ_1 and Δ_2. Since ideally the gain at the input of a comparator is irrelevant, this system produces outputs identical to those in the 2-1 architecture depicted in Figure 2.13, provided that [4]

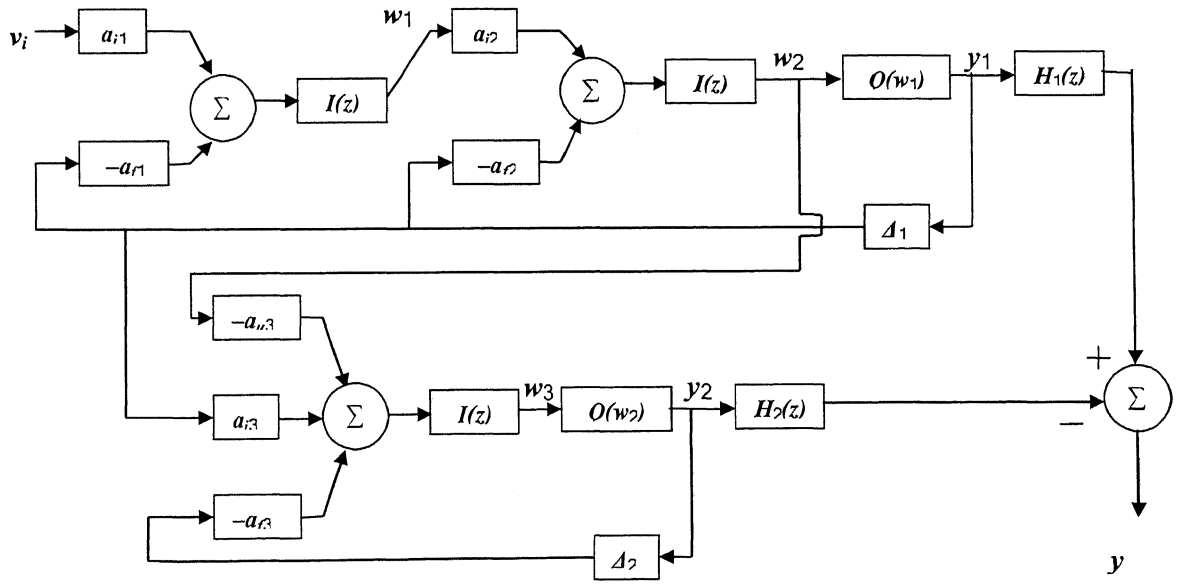


FIGURE 3.2 IDEAL 2-1 MASH ΣΔ MODULATOR ARCHITECUTRE

$$x = \frac{a_{i1}}{a_{f1}\Delta_1} v_i \tag{3.3}$$

$$b = \frac{a_{f2}}{a_{f1}a_{i2}} \tag{3.4}$$

$$\beta = \frac{a_{f1}a_{i2}a_{u3}}{a_{f3}} \frac{\Delta_1}{\Delta_2} \tag{3.5}$$

$$\lambda = \frac{a_{i3}}{a_{f1}a_{i2}a_{u3}} \tag{3.6}$$

where I(z) is given by Eq. (2.12). While Figure 3.2 shows the basic form of the implementation of a 2-1 architecture, real analog circuit blocks do not precisely perform their ideal function. The reminder of this chapter discusses of studying the effect of non-idealities in the modulator building blocks and how this can be implemented in Matlab, Simulink [30], to determine the circuit topologies that best meet the performance requirements of the modulator.

3.3 ΣΔ MODULATOR NONIDEALITIES

This section focuses on various circuit imperfections which can degrade the performance of the ΣΔ modulator. Both Switched-capacitor and continuous time integrators have been used in the design of high-resolution modulators. The advantages of using sampled data modulator over continuous modulator are discussed in section 2.4. So, we considered a SC ΣΔ modulator in this section. The most significant non-idealities are modeled in this section [12].

To understand the affects of different non-idealities on the performance of a ΣΔ modulator, we considered a first-order SC ΣΔ modulator which is shown in Figure 3.3. The modulator consists of an input sampler, a SC integrator, a quantizer and a feedback D/A converter. The non-idealities which we considered are clock jitter at the input sampler, thermal noise by switches in SC integrator and operational amplifier non-idealities like noise, finite DC gain, bandwidth, slew rate and saturation voltages.

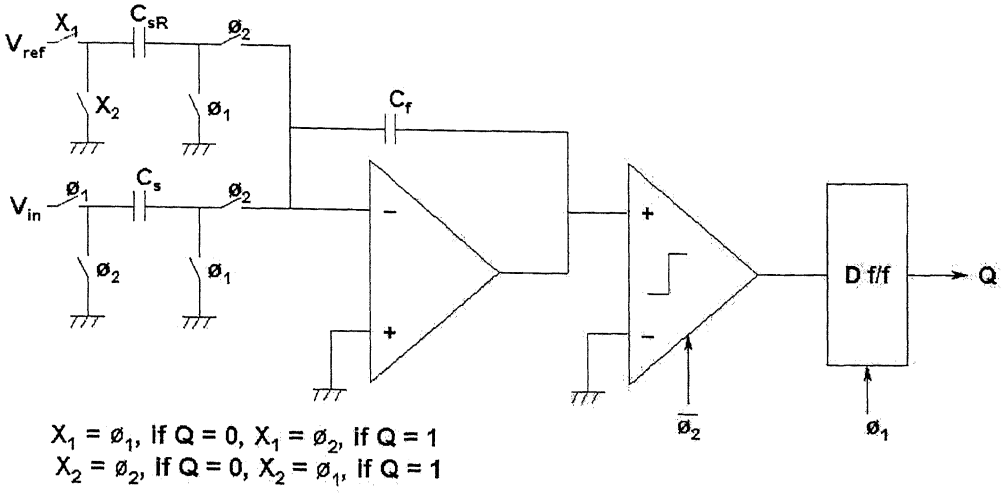


FIGURE 3.3 SCHEMATIC OF AN SC FIRST-ORDER ΣΔ MODULATOR

3.3.1 CLOCK JITTER

The operation of an SC circuit depends on complete charge transfers during each of the clock phases. Once the analog signal has been sampled, the SC circuit is a sampled-data system where variations of the clock period have no direct effect on the circuit performance. If the on-chip sampling circuitry is ideal, the sampling operation introduces errors due to the impurity of the external sampling clock. The jitter of the clock signal changes the time at which the sample is taken and therefore introduces errors. Therefore, the effect of clock jitter on an SC circuit is completely described by computing its effect on the sampling of the input signal [15][10].

Clock jitter results in a non-uniform sampling time sequence, and produces an error which increases the total error power at the quantizer output. Figure 3.3 shows a SC integrator. During clock phase Φ_1, the input signal is sampled on the sampling capacitance C_S and clock-jitter influences the sampled voltage. During clock phase Φ_2, a charge transfer takes place from C_S to C_F to perform the integration function. Since the settling error of this charge transfer has to be very small in order not to degrade the performance of the ΣΔ modulator. The

magnitude of this error is a function of both the statistical properties of the jitter and the modulator input signal.

When a sinusoidal input signal with amplitude A_i and frequency f_{in} is applied to the sampling block, the error due to the clock-jitter is given by

$$\Delta v_i = v_i(nT_S + \Delta T) - v_i(nT_S) \approx 2\pi f_{in} A_i \cos(2\pi f_{in} nT_S)\Delta T = \Delta T \frac{d}{dt} v_i(nT_S) \qquad (3.7)$$

where ΔT is the uncertainty of the sampling instance, T_S is the sampling period and nT_S is the ideal sampling moment. The sampling frequency f_S equals $1/T_S$. When the sampling uncertainty ΔT is assumed to be uncorrelated Gaussian random process with a standard deviation of $\sigma_{\Delta T_S}$ and a mean value of zero, the sampling error has a white spectrum with a bandwidth of. Hence the resultant error has uniform power spectral density (PSD) from 0 to $f_S/2$, with a total power given by

$$\sigma^2_{\Delta v} = \frac{(2\pi f_{in} A_i)^2}{2} \sigma^2_{\Delta T} \qquad (3.8)$$

Since the sampling error has a white spectrum and a ΣΔ modulator is oversampled, only a part of the sampling error will fall inside the signal band. The in-band power of the sampling error is given by

$$N_{jitter} = \frac{(2\pi f_{in} A_i)^2}{2} \frac{\sigma^2_{\Delta T}}{OSR} \le \frac{(\pi f_S A_i)^2}{2} \frac{\sigma^2_{\Delta T}}{OSR^3} \qquad (3.9)$$

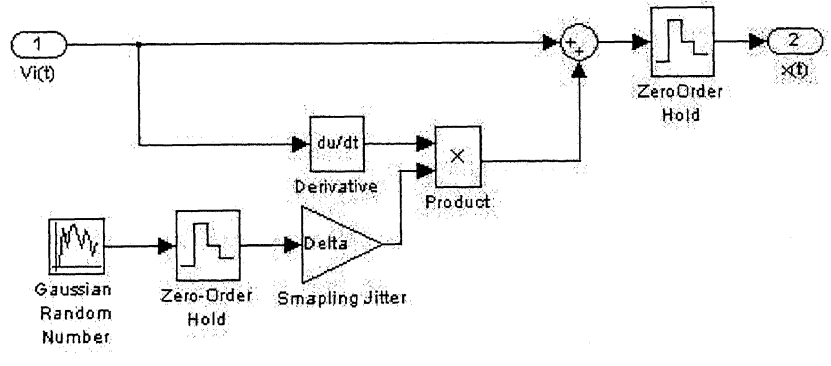


FIGURE 3.4 SAMPLING JITTER MODEL

The SNR is given by Eq. 3.10 which improves by the third power of the oversampling ratio (OSR).

$$SNR_{jitter} = \frac{(OSR)^3}{(\pi f_S \sigma_{\Delta T})^2} \tag{3.10}$$

The behavioral model of the above non-ideality is shown in Figure 3.4, which implements the Eq. (3.7) in Matlab SIMULINK [30]. The input signal $v_i(t)$ and its derivative (du/dt) are continuous-time signals. They are sampled with sampling period of T_S by a zero-order hold. Above we assumed that sampling uncertainty is a Gaussian random process with a standard deviation of $\sigma_{\Delta Ts}$. This can be implemented by using a random number sequence source with Gaussian distribution having zero mean and unity standard deviation. In the Figure 3.4, the random number generator, zero order hold circuit and the gain block delta introduces the sampling uncertainty. Hence the total error power will be reduced by the OSR as shown Eq. (3.9) and (3.10).

3.3.2 THERMAL NOISE OF SAMPLING SWITCHES

The most important noise sources affecting the operation of an SC ΣΔ modulator are the thermal noise associated to the sampling switches and the intrinsic noise of the operational amplifiers [15].

Thermal noise is caused by the random fluctuation of carriers due to thermal energy and is present even at equilibrium. Thermal noise has a white spectrum and wideband, limited only by the time constant of the switched capacitors or the bandwidth of the operational amplifiers. Considering the Figure 3.4, the sampling capacitor C_S is in series with finite resistance R_{on} of a sampling switch periodically opens and samples a noise voltage onto C_S. The resistance R_{on} is depends on the type of switch. If NMOS transistor is used as a switch, then R_{on} is given by Eq. (3.11) , for PMOS transistor R_{on} is given by Eq. (3.12) and for CMOS transistor R_{on} is given by Eq. (3.13)

$$R_{onN} = \frac{1}{K_{Pn}\left(\frac{W}{L}\right)_n \left((v_G - V_{Tn}) - \frac{v_S + v_D}{2}\right)} \tag{3.11}$$

$$R_{onP} = \frac{1}{K_{Pp}\left(\frac{W}{L}\right)_p \left(\frac{v_S + v_D}{2} - (v_G - V_{Tp})\right)} \tag{3.12}$$

$$R_{onCMOS} = (R_{onN} // R_{onP}) \tag{3.13}$$

Hence the switch can be modeled as a resistor having a noise source in series with a power source equal to the Johnson noise $4kTR_{on}\Delta f$. The total noise power can be found by evaluating the integral [10]

$$e^2_T = \int_0^\infty \frac{4kTR_{on}}{1+(2\pi f R_{on}C_S)^2} df = \frac{kT}{C_S} \tag{3.14}$$

where k is the Boltzmann's constant, T is the absolute temperature. From the Eq. (3.14), we note that the thermal noise is generated by the resistor but the noise power depends only on the capacitor. The switch thermal noise voltage e_T is then superimposed to the input voltage $x(t)$ leading to

$$\begin{aligned} y(t) &= [x(t) + e_T(t)]b \\ &= \left[x(t) + \sqrt{\frac{kT}{C_S}}n(t)\right]b \\ &= \left[x(t) + \sqrt{\frac{kT}{bC_f}}n(t)\right]b \end{aligned} \tag{3.15}$$

where $n(t)$ denotes a Gaussian random process with unity standard deviation, while $b=C_S/C_f$ is the coefficient of the integrator.

The implementation of thermal noise non-ideality given in Eq. (3.15) using Simulink is shown in Figure 3.5. In this model shown in Figure 3.5 the Gain input is the integrator coefficient b and the function $f(u)$ evaluates the e_T which given in Eq. (3.14). The integrators of an SC ΣΔ modulator may include more than one SC input branch, each contributing to the total noise power. For each input branch of the SC summing integrator we should modeled with a separate kT/C noise block, including the proper gain input coefficient b.

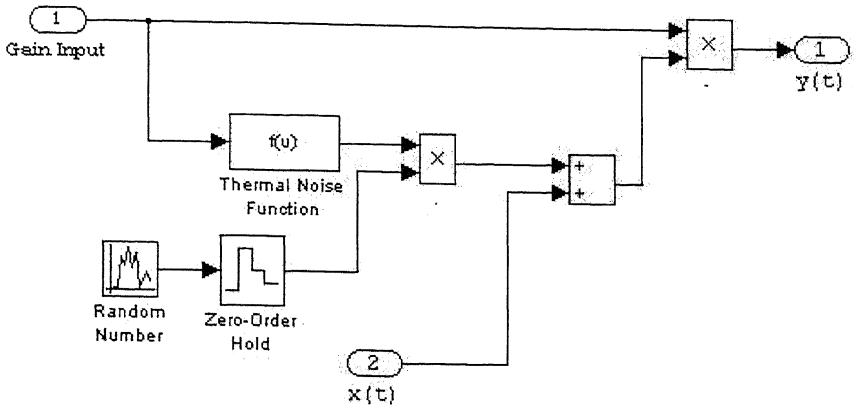


FIGURE 3.5 MODELING SWITCHES THERMAL NOISE (*KT/C*)

3.3.3 OPERATIONAL AMPLIFIER NOISE

The block diagram of an ideal integrator is shown in Figure 3.6. The z-domain transfer function of the integrator shown in Figure 3.3 is given by

$$H_I(z) = \frac{C_S}{C_F}\frac{z^{-1}}{1-z^{-1}} = b\frac{z^{-1}}{1-z^{-1}} \tag{3.16}$$

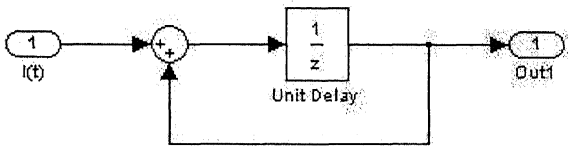


FIGURE 3.6 IDEAL INTEGRATOR

Two main sources of noise in switched-capacitor integrator are thermal noise from the amplifier and switches, and flicker noise from the operational amplifier. Here we neglected the effect of flicker noise (1/f) on the circuit. The noise appearing at the output of a SC circuit is due to the two different propagation methods, direct broad band noise and sample-hold noise. The direct broad band noise is due to the noise sources with direct coupling to the output

during at least one clock phase. The sampled noise component is due to the sampling of the direct broadband noise on the sampling capacitance at the end of the sampling and integration phase. Since the bandwidth of the broadband is much larger than the sampling frequency, noise aliasing takes places during the sample operation. Due to this, the flicker or $1/f$ noise will be submerged by this aliased broadband noise. Therefore, the flicker noise is neglected in our analysis [10].

The noise generated by the switches can be represented by a white noise source with a power spectral density of $4kTR_1$ and $4kTR_2$ for the switches during sampling and integration phase, respectively. The noise of a reference voltage can also be represented by an equivalent hypothetical resistor R_{Vref}. This results in a power spectral density of $4kTR_{Vref}$. Finally, the noise of the operational amplifier can be represented as

$$V_n^2 = \frac{8kT}{3g_m}\gamma \tag{3.17}$$

where g_m is the operational amplifier transconductance and γ is the noise excess factor of the amplifier, which is given by the ratio of the equivalent input noise of the amplifier to the noise of the input transistor.

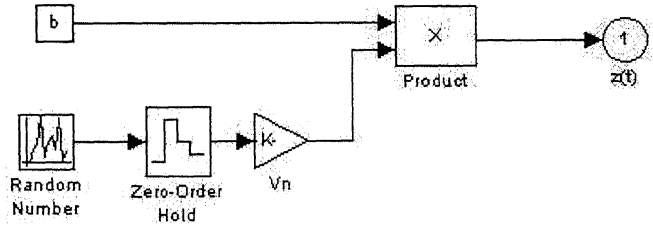


FIGURE 3.7 OP-AMP NOISE BLOCK

Simulink model for the operational amplifier noise block is shown in Figure 3.7. In the above diagram V_n represents the *rms* noise voltage of the operational amplifier referred to the integrator output. Figure 3.8, shows the complete Simulink model of a noisy integrator, while considering both the thermal noises due to the sampling switches and due to the operational amplifier.

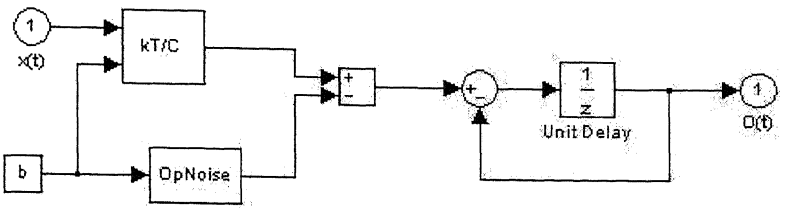


FIGURE 3.8 NOISY INTEGRATOR MODEL

3.3.4 OPERATIONAL AMPLIFIER NON–IDEALITIES

The transfer function of the ideal integrator is given in Eq. (2.12). The behavioral model of an ideal integrator is shown in Figure 3.6. Analog circuit implementation of the integrator deviates from this ideal behavior due to several nonideal effects. One of the major causes of performance degradation of SC ΣΔ modulators is the incomplete transfer of charge in the SC integrators. Due to the influence of several nonidealities, the performance of a practical implementation of a ΣΔ modulator can be significantly worse than the values predicted by the simulations of ideal ΣΔ modulators in section 3.2. This nonideal effect is a consequence of the operational amplifier nonidealities, namely finite gain and bandwidth, slew rate and saturation voltages [10].

3.3.4.1 DC GAIN

The DC gain of the ideal integrator is infinite as given in Eq. (2.12). In practice, the actual gain is limited by the operational amplifier open loop gain A. Due to this, a fraction of the previous output of the integrator is added to each new input sample. The limited dc gain of the integrator increases the in-band noise. Considering the SC integrator shown in Figure 3.3, the operational amplifier can be represented as a voltage controlled voltage source with gain A. By applying the principles of charge conservation and Kirchoff's laws and combining the equations for the sampling and integration phase, the output of the integrator at the end of the sampling phase can be calculated as

$$H(z) = \frac{C_S}{C_F} \frac{\rho_2 z^{-1}}{\left(1 - \frac{\rho_2}{\rho_1} z^{-1}\right)} \tag{3.18}$$

where ρ_1 and ρ_2 are the closed loop static errors during the sampling and the integration phase and they are given by

$$\rho_1 = \frac{A.f_{dc1}}{1 + A.f_{dc1}} \tag{3.19}$$

$$\rho_2 = \frac{A.f_{dc2}}{1 + A.f_{dc2}} \tag{3.20}$$

$$f_{dc1} = 1 \tag{3.21}$$

$$f_{dc2} = \frac{C_F}{C_S + C_{SR} + C_F} \tag{3.22}$$

where f_{dc1} and f_{dc2} are the capacitive feedback factors during the sampling and integration phase respectively. Here we neglected the parasitic capacitances of the amplifier. Substituting the equations (3.19) to (3.22) in Eq. (3.18), the transfer function can be written as

$$H(z) = \frac{z^{-1}}{1 - \alpha z^{-1}} \tag{3.23}$$

where,

$$\alpha \cong \frac{AC_F}{C_S + C_{SR} + AC_F} \tag{3.24}$$

The DC gain of the integrator now becomes

$$H_O = H(1) = \frac{1}{1-\alpha} = \frac{C_S + C_{SR} + AC_F}{C_S + C_{SR}} \tag{3.25}$$

In practical implementation of an amplifier, the gain is not the same for all values of the output voltage. Hence a higher value of gain is necessary to reduce the distortion caused by this effect. The Simulink model of this nonideality is shown in Figure 3.9. The integrator part in this figure shows the implementation of Eq. (3.23), where the gain block in the feedback loop is equal toα.

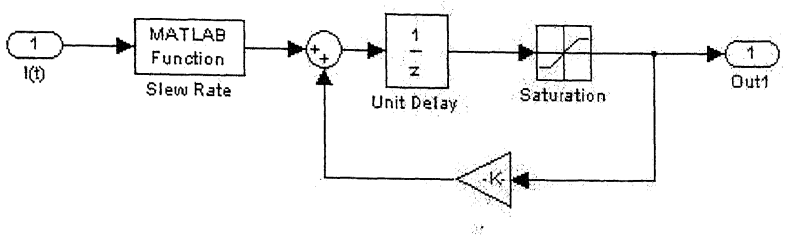


FIGURE 3.9 REAL INTEGRATOR MODEL

3.3.4.2 BANDWIDTH AND SLEW RATE

Another important nonideal effect in the SC integrators is the slewing of the amplifier. Finite BW and slew rate (SR) in SC circuits lead to a nonideal transient response within each clock cycle, thus producing an incomplete or inaccurate charge transfer to the output at the end of the integration period. Incomplete settling of the integrator outputs due to finite bandwidth of operational amplifiers translates into an equivalent gain error as long as the settling process is linear. Considering the integrator shown in Figure 3.3, whose transient response during each sampling period is characterized by a single-pole exponential given by

$$\Delta V_{out} = V_{in}(1-e^{-T_S/\tau}) \tag{3.26}$$

where, T_S is the sampling period and τ is the settling time constant, which is given by

$$\tau = \frac{1}{2\pi GBW} \tag{3.27}$$

where, GBW is the unity gain bandwidth product.

In the n^{th} integration period Φ_2 is on, between $(nT_S - T_S/2)$ and (nT_S). The evolution of the output node during this integration period is given by

$$v_o(t) = v_o(nT_S - T_S) + \alpha V_S\left(1-e^{-t/\tau}\right) \tag{3.28}$$

where, $V_S = V_{in}(nT_S - T_S/2)$, α is the integrator leakage which is given in Eq.(3.24). The slope of the curve reaches its maximum value when $t=0$, resulting in

$$\left.\frac{d}{dt}v_o(t)\right|_{max} = \alpha\frac{V_S}{\tau} \tag{3.29}$$

If the value specified in Eq. (3.29) is lower than the operational amplifier SR, then no SR limitation appears and the evolution of v_o is described by Eq. (3.28) during the whole clock period (until $t=T_S/2$).

If the value specified by Eq. (3.29) is larger than SR, then the operational amplifier is in slewing. Therefore, the first part of transient of v_o is linear with slope SR for ($t<t_0$). Then the output equations for this condition are given by

$$v_o(t) = v_o(nT_S - t_S) + SR.t \qquad (t \le t_0) \qquad (3.30)$$

$$v_o(t) = v_o(t_o) + (\alpha V_S - SRt_0)\left(1 - e^{-\frac{t-t_0}{\tau}}\right) \qquad (t > t_0) \qquad (3.31)$$

Imposing the condition for the continuity of the derivatives of Eq.'s (3.30) and (3.31) in t_0, we obtain

$$t_0 = \frac{\alpha V_S}{SR} - \tau$$

For $t_0 \ge T_S/2$, the output voltage is given in Eq. (3.30) holds for the whole clock period.

In the Simulink model shown in Figure 3.9, the Matlab function block implements the above equations to calculate the value reached by $v_o(t)$ at time T_S, which will be different from V_S due to the gain, BW and SR limitations of the operational amplifier. The SR and BW limitations produce harmonic distortion reducing the total SNR of the ΣΔ modulator.

3.3.4.3 SATURATION VOLTAGES

The saturation voltages of the operational amplifier have impact on the output signal of the SC integrator. The dynamic range of signals in a ΣΔ modulator is a major concern. It is therefore important to take into account the saturation levels of the operational amplifier. This is implemented in Simulink using a saturation block inside the feedback loop of the integrator as shown in Figure 3.9.

3.4 IMPROVEMENTS TO BEHAVIORAL MODEL

3.4.1 OP-AMP DC GAIN

In the above explained behavioral model, while modeling the operational amplifier finite DC gain, we are taken an assumption that parasitic capacitances of the amplifier when compare to the sampling capacitances C_S, C_{SR} and C_F. In practical, the intrinsic capacitances have comparable values with respect to the sampling capacitances [15].

Consider the SC integrator shown in Figure 3.3, let the parasitic capacitances of the amplifier be C_P and C_L at input and output pins of the amplifier, respectively. The transfer function of the integrator is same as in Eq. (3.18) but the values of ρ_1 and ρ_2 changes due to the feedback factors given by

$$f_{dc1} = \frac{C_F}{C_F + C_P} \tag{3.32}$$

$$f_{dc2} = \frac{C_F}{C_S + C_{sR} + C_F + C_P} \tag{3.33}$$

and the value of α is approximately given by

$$\alpha \approx \frac{A(C_F + C_P)}{A(C_F + C_P) + C_S + C_{sR}} \tag{3.34}$$

In the Simulink model of the integrator block the value of the gain block is to be changed with the value of α given in Eq. (3.34).

3.4.2 SATURATION VOLTAGES

In the implementation of the higher order ΣΔ modulators, only the nonidealities of the first integrator are considered since their effects are not attenuated by the noise shaping. Other are implemented using ideal blocks. In [12], they had implemented a second order ΣΔ modulator. They considered the second integrator as an ideal integrator shown in Figure 3.6. While doing simulations we found that the output of the second integrator has no bound limits. To overcome this problem, we introduced a saturation block in the ideal integrator model as shown in Figure 3.10. The results of this model are discussed in the next section.

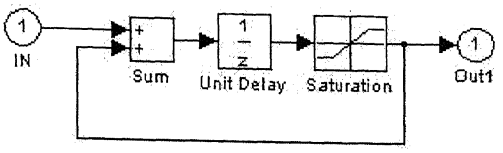


FIGURE 3.10 IDEAL INTEGRATOR BLOCK WITH SATURATION LIMITS

3.5 SECOND ORDER ΣΔ MODULATOR

By using the above behavioral model, a second order ΣΔ modulator is implemented. The block diagram for the second order ΣΔ modulator is shown in Figure 3.11. The design parameters used for the simulations is shown in Table 3.1.

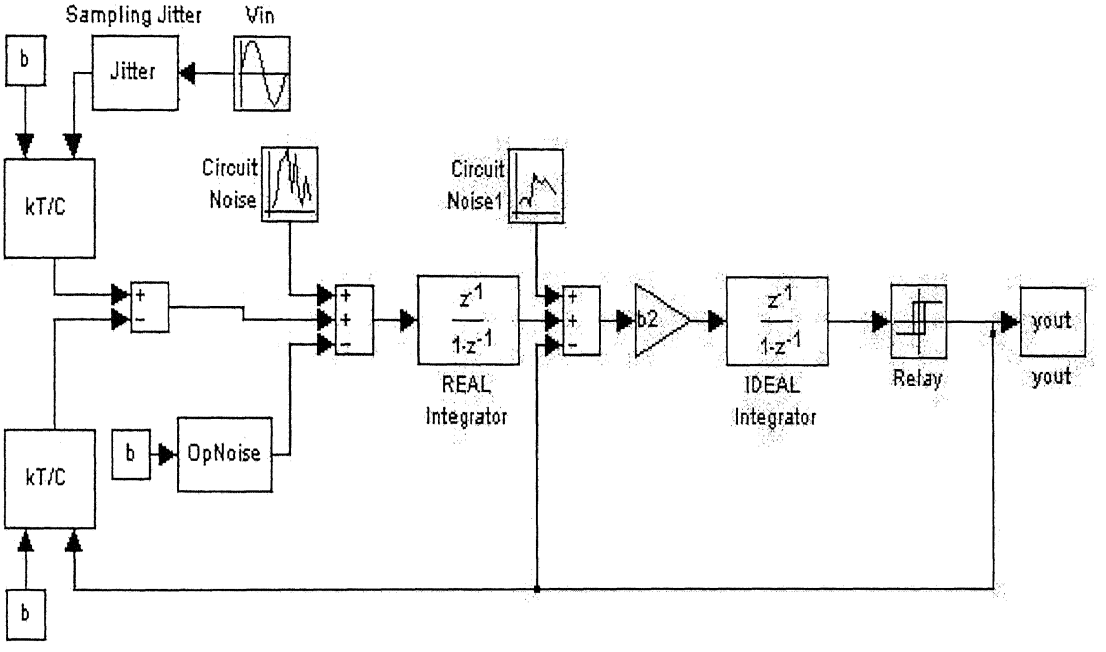


FIGURE 3.10 SECOND ORDER ΣΔ MODULATOR BEHAVIORAL MODEL

Table 3.2 compares the SNR obtained from the model given in [12], with our improved model. Measurement results of the integrated prototype second order modulator is also mentioned in this table. From this table, it can be easily shown that our behavioral model is getting results almost nearer to the practical values.

Parameter	*Value*
Signal Bandwidth (*BW*)	100 Hz
Sampling Frequency (f_S)	50 KHz
Oversampling Ratio (*R*)	250
Number of samples considered (*N*)	65536
Integrator Coefficients	$b = b_2 = 0.5$

TABLE 3.1 DESIGN PARAMETERS OF THE SECOND–ORDER LOW–PASS ΣΔ MODULATOR MODEL

	Ideal Modulator	Behavioral Model proposed in [12]	Our Model	Practical Results [12]
SNR (dB)	99.1	91.6	90.7	90.2
Resolution (bits)	16.17	14.94	14.8	14.69

TABLE 3.2 COMPARISON OF IDEAL AND NON-IDEAL SECOND- ORDER ΣΔ MODULATOR

The value of sampling capacitance used in simulation is 2.5*pF* and parasitic capacitance value is 0.5*pF*. The SR and BW values used in the simulation are $4V/\mu s$ and 11.25 *MHz*. Saturation voltage of the integrator is 1.5V. The gain of the amplifier is taken as 60 *dB*. The input referred operational amplifier noise is given as 73 μV_{rms}. The value of the sampling uncertainty is taken as 16 *ns*. Table 3.3 compares the SNDR obtained from the simulation of the model proposed in [12], with our improved model, when one single nonideality is considered.

ΣΔ Modulator Parameter	*SNR [dB] of Model [12]*	*SNR [dB] of our model*
Sampling Jitter	98.8	98.45
Switches Thermal Noise	94.0	93.24
I/P-referred op-amp Noise	94.8	93.74
Finite DC gain	98.9	96.8
Finite Bandwidth	99.1	97.69
Slew Rate	99.1	97.69
Saturation Voltages	99.1	97.69

TABLE 3.3 COMPARISON OF SNR WITH OUR PROPOSED MODEL

3.6 SUMMARY

This chapter reviews the different nonidealities that affects the performance of the ΣΔ modulator and developed a behavioral model which takes account of most of the nonidealities. Modulator building blocks and the signal scaling for the building blocks are first presented. The different nonideal parameters and their effect on the ΣΔ modulator are discussed. Their behavioral model implementation using Matlab, Simulink tool is presented. The effect of parasitic capacitance is discussed and its implementation using Simulink is presented. Finally, a second-order ΣΔ modulator is taken and compared the SNR of our proposed model with the model given in [12], taking several non-idealities is presented.

Chapter 4

SC INTEGRATOR AND AMPLIFIER DESIGN

4.1 INTRODUCTION

Switched-capacitor (SC) integrators are the key circuit building block in a sigma-delta modulator. This chapter explores design tradeoffs and power-optimization strategies for key circuit blocks which are at the heart of the sigma-delta ($\Sigma\Delta$) modulator. These include switched-capacitor integrators, operational transconductance amplifiers (OTA), bias networks, comparators, digital output buffers, and two-phase clock generation circuitry. From the circuit level specification, choice of operational amplifier topology is investigated. Once the amplifier topology is fixed, quantities such as dc gain, settling time, thermal noise and slew rate may be analyzed.

This chapter begins with the basic operation of a fully differential SC integrator. Next section addresses different operational amplifier topologies that are used in the designing of the SC integrator. In the next section, a fully differential telescopic cascade operational amplifier and its parameters are analyzed. Finally, the design of comparator, two phase clock generator and output buffer are discussed.

4.2 INTEGRATOR DESIGN

Differential implementation of an integrator has several advantages when compare to the single ended design. The clock feedthrough and charge injection of the switches cancels better since these errors are considered as a common mode signal. The settling improves since the extra pole due to differential to single ended conversion in the OTA is avoided. A differential implementation significantly reduces even order harmonic distortion components due to the symmetry and offers a better power supply rejection ratio. The main draw back for differential circuits is the requirement for a common mode feedback. In SC integrator, this can be implemented by dynamic common mode feedback circuit which has a negligible power consumption and area overhead.

The 2-1 cascaded ΣΔ modulator architecture comprises three SC integrators. Figure 4.1 illustrates the first integrator in the cascade. The integrator is implemented in a fully-differential configuration and employs a two-phase non-overlapping clock, the latter of which is shown in Figure 4.2. The input is sampled during phase 1 (Φ_1 and Φ_{1d}). During phase 2, the charge is transferred from the sampling capacitors (C_S and C_{ref}) to the integrating capacitor (C_F). At the same time, depending on the output value, the appropriate DAC reference level is applied by closing either switches labeled Φ_{2d1} or Φ_{2d2}.

The integrator employs the bottom-plate sampling technique to minimize signal dependent charge-injection [6],[7],[8],[9]. This is achieved through delayed clocks: Φ_{1d}, Φ_{2d1} and Φ_{2d2}. When switches labeled, Φ_1 are first turned off, the charge injection from those switches remains, to a first order, independent of the input signal. Because one of plates is now floating, turning off switches labeled Φ_{1d} shortly after does not introduce charge-injection errors.

The general transfer function for the standard SC integrator shown in Figure 4.1, is given by

$$\frac{V_{OUT}}{V_{IN}}(z) = \frac{C_S}{C_F}\frac{z^{-1}}{1-z^{-1}} \tag{4.1}$$

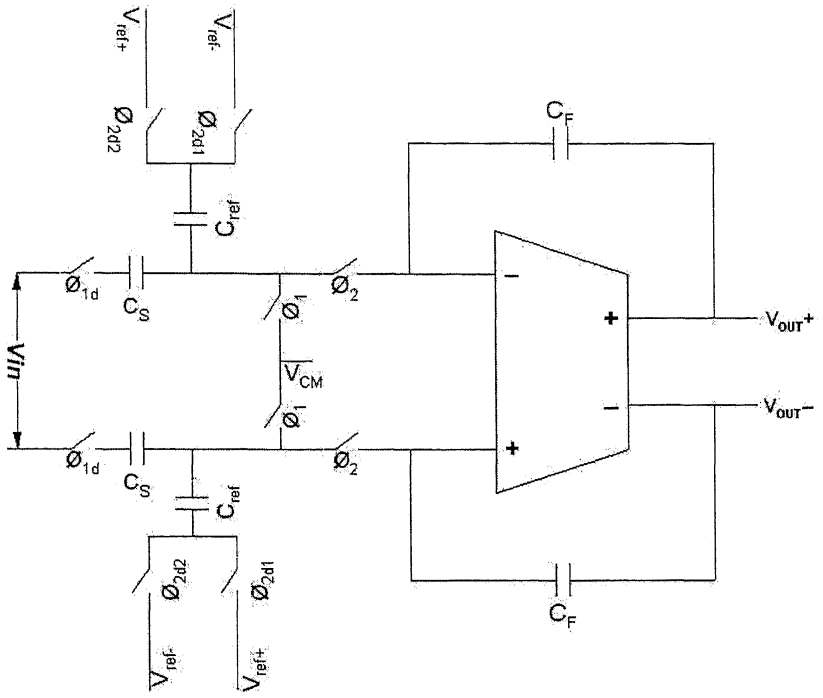


FIGURE 4.1 FULLY DIFFERENTIAL SWITCHED CAPACITOR INTEGRATOR

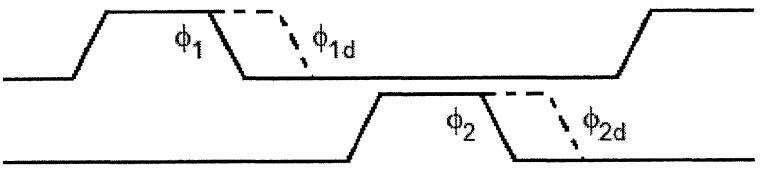


FIGURE 4.2 TWO-PHASE NON-OVERLAP CLOCK

The DAC feedback path is created by the switches connected to V_{REF+} and V_{REF-}. Their switch control signals (Φ_{2d1} and Φ_{2d2}) are cross coupled in order to appropriate sample the differential DAC signal through C_{REF}.

4.2.1 SWITCHES

Linearity is an important factor in the design of the switches. From Figure 4.3, it is desirable to operate in a region where the on resistance of the switch is

independent of the input voltage. The switches used in the integrator are implemented with complementary MOS devices because the DC voltages are biased at mid-supply. Alternatively, gate boasting techniques using charge pumps may be employed to keep a constant on resistance [6],[8]; however the process for which this experimental prototype is designed does not permit voltages above V_{DD}.

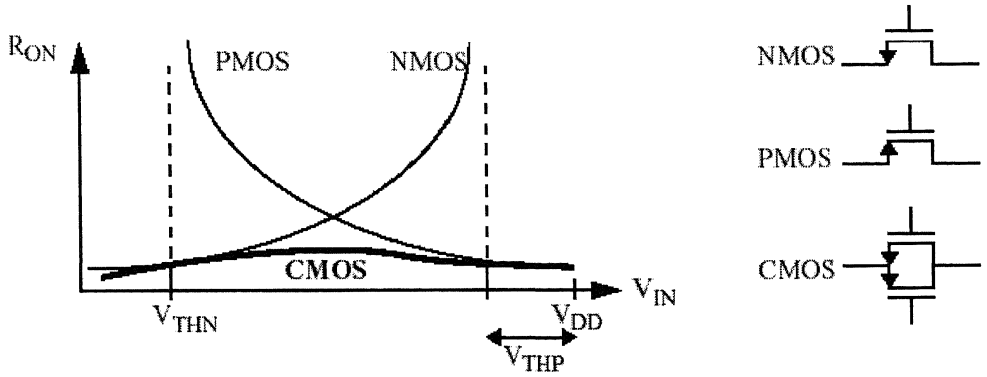


FIGURE 4.3 SWITCH ON–RESISTANCE AS A FUNCTION OF INPUT VOLTAGE

In CMOS switches, the sizing of the NMOS and PMOS devices is critical. The parallel combination of the NMOS and PMOS devices yields an effective resistance given by Eq. (3.13), can be written as

$$R_{onCMOS} = \left[\mu_N C_{OX} \left(\frac{W}{L} \right)_N (V_{GSN} - V_{TN}) + \mu_P C_{OX} \left(\frac{W}{L} \right)_P (V_{SGP} - |V_{TP}|) \right]^{-1} \tag{4.2}$$

For linearity reasons, the input switches, labeled Φ_{1d}, Φ_{2d1} and Φ_{2d2} in Figure 4.1, should be designed for equal impedances. This means the PMOS should be made larger than the NMOS by a factor equal to the ratio μ_B/μ_P, as shown below.

$$\frac{\left(\frac{W}{L} \right)_P}{\left(\frac{W}{L} \right)_N} = \frac{\mu_N}{\mu_P} \tag{4.3}$$

The bottom-plate switches, labeled Φ_1 and Φ_2 in Figure 4.1, should be designed for a first-order cancellation of charge-injection errors. The error is given by

$$\Delta V_{OUT} = -\frac{1}{2}\cdot\frac{(Q_{chan})_N}{C_S} + \frac{1}{2}\cdot\frac{(Q_{chan})_P}{C_S}$$
$$= -\frac{1}{2}\cdot\frac{C_{OX}}{C_S}\{W_N L_N(V_{DD} - V_{IN} - V_{THN}) - W_P L_P(V_{IN} - V_{THP})\} \quad (4.4)$$

For a partial cancellation of charge-injection error, the NMOS and PMOS devices should be designed to have equal sizes.

$$W_N L_N = W_P L_P \quad (4.5)$$

The fully-differential configuration of the integrator further mitigates the effects of signal-dependent charge injection. In addition to sizing the switches for linearity and charge-injection reasons, the sampling network also needs to be designed for sufficient bandwidth. Increasing the switch sizes decreases the resistance but increases the parasitic capacitance of the network. An optimum value of the switch size which yields a minimum R-C time constant can be determined.

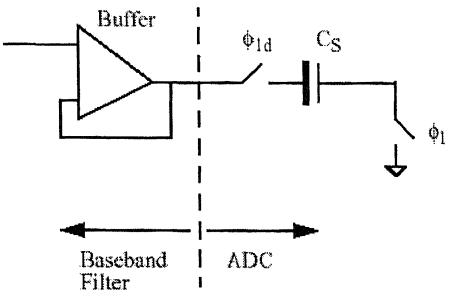
4.2.2 SAMPLING AND INTEGRATING CAPACITORS

The sizes of the sampling and integrating capacitors are dictated by the noise requirements [7],[8],[9]. The ideal input-referred thermal noise of the integrator is given by

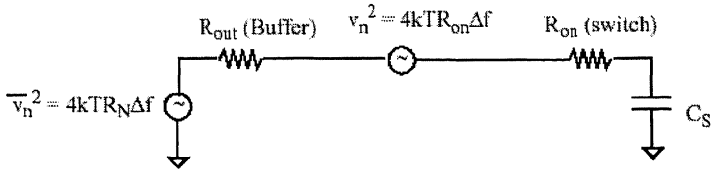
$$P_{N,ideal} = \frac{4kT}{C_S} \quad (4.6)$$

Ideally, during phase 1, a noise sample with variance $2kT/C_S$ (kT/C_S on each of the differential path) is captured across the sampling capacitors when the switches labeled Φ_1 are open. Another $2kT/C_S$ is sampled across the sampling capacitors during phase 2. However, because of nonideal effects described below, the total input-referred noise will be larger than that predicted by Eq, (4.6).

The switches labeled Φ_1 are not driven by an ideal input voltage source; rather, it is driven by a buffer stage in the preceding baseband filter, as shown in Figure 4.4(a). The simplified noise model is shown in Figure 4.4(b). The noise sampled across C_S during Φ_1 is therefore given by



(a)



(b)

FIGURE 4.4 (a) FILTER-TO-ADC INTERFACE (b) NOISE–MODEL DURING PHASE 1

$$P_{Nideal,\phi 1} = 4kT(R_N + R_{on})\Delta f.\left|\frac{1}{1+s(R_{out}+R_{on})C_S}\right|^2 \tag{4.7}$$

where,

$$R_N \approx \frac{2}{3}\frac{1}{g_{m,buffer}}$$
$$R_{out} \approx \frac{1}{g_{m,buffer}} \tag{4.8}$$

Because the noise resistance and output resistance of the buffer driving the sampling network are not the same, the result does not yield a simple kT/C value. Reorganizing the Eq. (4.7), the total input-referred noise power can be written as

$$P_{Nideal,\phi 1} = \frac{R_N + R_{on}}{R_{out} + R_{on}}.4kT(R_{out} + R_{on})\Delta f\left|\frac{1}{1+s(R_{out}+R_{on})C_S}\right|^2$$
$$= \frac{R_N + R_{on}}{R_{out} + R_{on}}.\frac{kT}{C_S} \tag{4.9}$$

During phase 2, due to thermal noise from the operational transconductance amplifier (OTA), when the switches labeled Φ_2 are open, then the noise captured across C_S can be greater than $2kT/C_S$. The OTA in-band flicker noise, when referred to the input of the integrator, simply adds on to the total input-referred noise power.

It is interesting to note that although the noise power is doubled in differential architectures, the input signal power is quadrupled. This results in a net gain of 3dB in dynamic range. Moreover, fully-differential integrators are more immune toward power-supply, common-mode and substrate-coupled noise.

$$DR = \frac{P_{IN}}{P_{Noise}} \tag{4.10}$$

Because of noise shaping, later integrators will have relaxed noise requirements. This suggests that the capacitors in later integrators in the cascade will be selected based on parasitic considerations rather than noise.

4.3 OPERATIONAL AMPLIFIER TOPOLOGY SELECTION

The operational amplifier requirements are most stringent for the first integrator in the cascade. Leak of first stage quantization noise demands an operational amplifier topology with dc gain of greater than 1000. This corresponds to a gain on the order of $(g_m r_o)^3$ and requires the use of a two-stage or three-stage nested-Miller amplifier. The amplifier must be able to settle fast at higher clock rates. This precludes the use of nested-Miller topologies which are significantly slower than two-stage amplifiers [10],[13],[17]. Amplifier thermal noise and kT/C noise must be small enough to achieve 14–bit resolution. The amplifier must also have adequate output swing. Output swing favors topologies with a common source second stage.

4.3.1 Candidate Operational Amplifier Topologies

Any two-stage amplifier with common source second stage and cascoded first stage can meet the specifications discussed in the previous section. Four

candidate topologies are shown in Figure 4.5 - Figure 4.8. The topologies differ in the type of compensation employed either standard Miller [6],[16] or cascode compensation [17], [18],[19]. The topologies also differ in whether the first stage of the amplifier is a folded-cascode or telescopic topology. If the first stage is a telescopic topology, then the common-mode voltage at the output of the first stage is not the same as the dc bias point required at the second stage input. As a result, a switched-capacitor dynamic level-shift is provided between the two stages of the amplifier in Figure 4.6 to independently set the first stage output common-mode level and second stage input dc bias. The level-shift is biased in identical manner to a switched-capacitor common mode feedback circuit. In Figure 4.8, the second stage is made fully differential instead of a quasi-differential common source stage for a number of reasons. Having a tail-current device eliminates the need for a power-hungry inversion stage for the common-mode feedback amplifier. The fully-differential second stage amplifier also eliminates the need for a dynamic level shift between the output of the first stage and the input of the second stage [18]. In addition, this fully-differential topology improves the power-supply rejection ratio (PSRR) and the common-mode rejection ratio (CMRR).

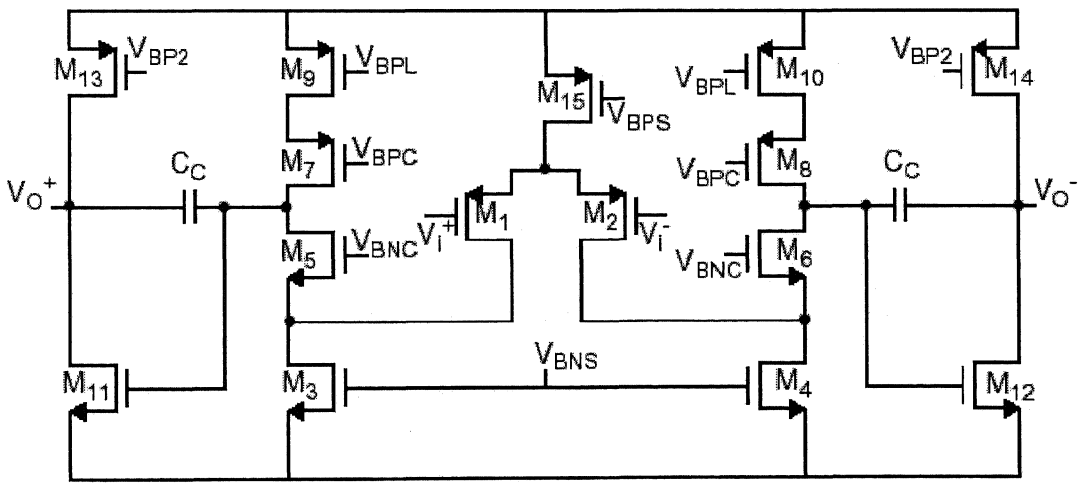


FIGURE 4.5 TWO STAGE FOLDED CASCODE OTA WITH MILLER COMPENSATION

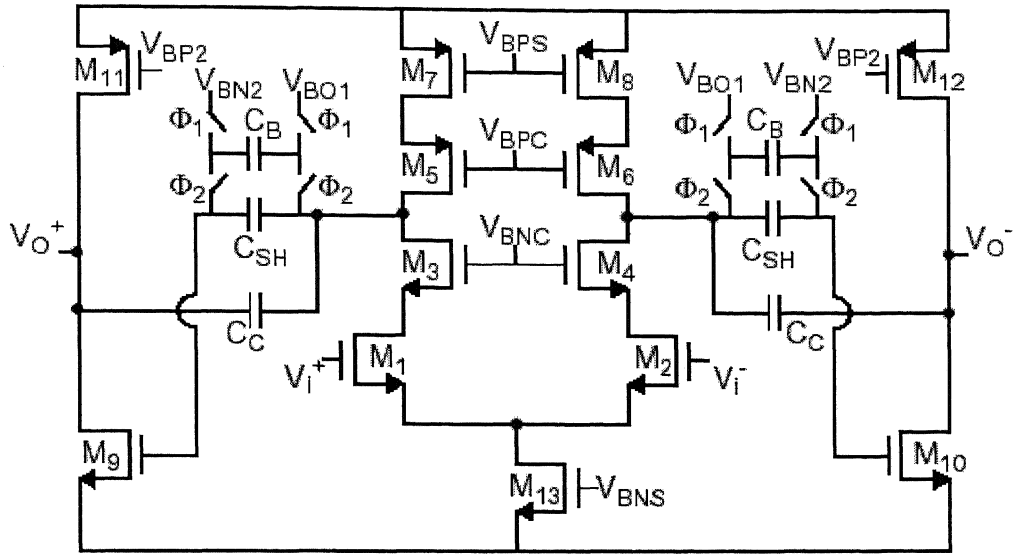


FIGURE 4.6 TWO STAGE TELESCOPIC OTA WITH MILLER COMPENSATION

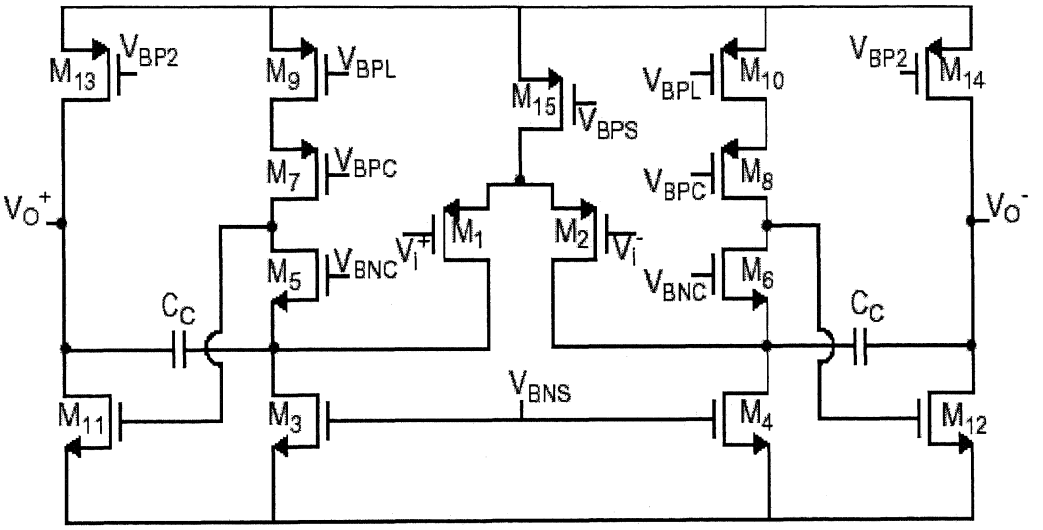


FIGURE 4.7 TWO STAGE FOLDED CASCODE OTA WITH CASCODE COMPENSATION

4.3.2 LOW-POWER OPERATIONAL AMPLIFIER CHARACTERISTICS

The objective is to select the lowest power operational amplifier topology from the candidates in Figure 4.5–Figure 4.8 by investigating desirable characteristics for low - power operation. Such desirable characteristics are:

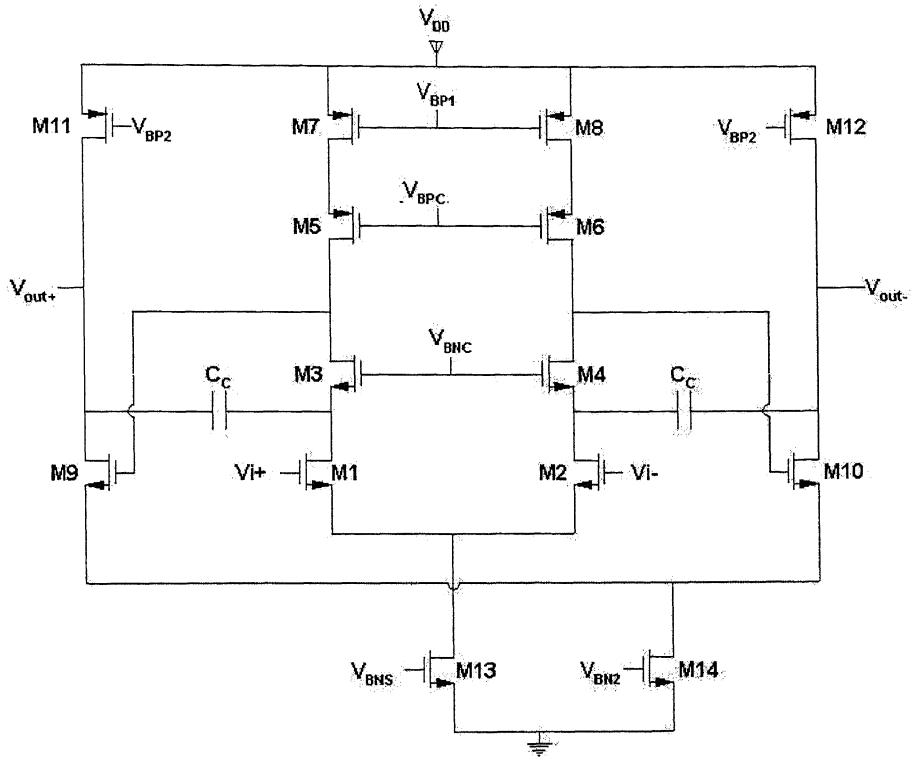


FIGURE 4.8 TWO STAGE TELESCOPIC OTA WITH CASCODE COMPENSATION

1) minimum number of current legs, 2) minimum number of devices which contribute significant thermal noise, 3) all NMOS signal path for maximum speed, and 4) a maximum bandwidth compensation loop [11].

Since minimizing power dissipation amounts to minimizing the static bias current, one obvious approach is to minimize the number of current legs in an amplifier. For a fixed settling constraint and compensation scheme in the candidate two-stage amplifiers, an amplifier with fewer current legs will be lower power than an amplifier with more current legs. For a fully-differential two-stage amplifier, the minimum number of current legs is four. The amplifiers in Figure 4.6 and Figure 4.8 with telescopic first stage meet this constraint. Folding the first stage of the amplifier as in Figure 4.5 and Figure 4.7 increases the number of current legs to six. Thus, minimizing the number of current legs favors topologies with a telescopic front-end.

Since power and noise directly trade off, minimizing the number of devices in the amplifier which contribute thermal noise will reduce power dissipation. In a properly designed two-stage amplifier, thermal noise will be dominated by the first stage of the amplifier since the second stage noise will be attenuated by the first stage gain when referred to the input. For the telescopic first stage amplifiers in Figure 4.6 and Figure 4.8, four devices (M1, M2, M7 and M8) contribute significant amplifier thermal noise. This corresponds to an input device and active load device for each side of the fully-differential amplifier, the minimum number of devices for such a topology. The folded-cascode input stage topologies in Figure 4.5 and Figure 4.7 have six devices (M1, M2, M3, M4, M9 and M10) which contribute significant amplifier thermal noise. As a result, the topologies with telescopic first stage minimize the number of devices which contribute significant amplifier thermal noise.

NMOS devices are approximately 3 X faster than PMOS devices due to the difference between the mobilities of electrons and holes. As a result, amplifiers with all NMOS signal paths will be higher speed than amplifiers with PMOS devices in the signal path. Since speed and power directly trade off, a higher speed amplifier will dissipate less power for a fixed settling constraint. The telescopic first stage amplifiers in Figure 4.6 and Figure 4.8 have all NMOS devices (M1, M2, M3, M4, M9 and M10) in their signal paths while the folded-cascode input stage amplifiers in Figure 4.5 and Figure 4.7 have PMOS input devices. Note that the amplifiers with PMOS inputs will have the advantage of reduced 1/f noise which is especially important for low-frequency applications. Thus, the higher-speed of the telescopic cascaded amplifiers will result in a lower power solution.

Some form of compensation is required to maintain stability in a two-stage amplifier placed inside the feedback loop of a switched-capacitor integrator. The standard Miller compensation scheme places a pole-splitting capacitor between the output of the overall amplifier and the output of the first stage of the amplifier as shown in Figure 4.5 and Figure 4.6. This has the effect of creating a dominant low frequency pole and moving the second pole to a higher frequency which will ensure

amplifier stability when it is placed in a feedback loop. On the other hand, the cascode compensation scheme shown in Figure 4.7 and Figure 4.8 creates a dominant pole and two complex poles at higher frequency by placing a compensation capacitor between the amplifier output and first stage cascode node. This will also ensure amplifier stability when it is placed in a feedback loop. While both compensation schemes ensure stability, the cascode compensation scheme increases the speed of the amplifier as compared to the conventional Miller compensation scheme [20]. Since higher speed amplifier topologies will achieve lower power dissipation under a fixed settling constraint, the cascode compensation scheme is preferred.

4.3.3 OTA FOR THE 2–1 CASCADE SIGMA–DELTA MODULATOR

The amplifier topology in Figure 4.8 with telescopic front-end and cascode compensation is the best of the candidate topologies in Section 4.3.2 from a power dissipation perspective. This topology satisfies the four desirable characteristics for low-power operation: minimum number of current legs, minimum number of noise contributing devices, all NMOS signal path, and maximum bandwidth compensation loop. However, the relaxed 1/f noise constraints due to the 320 kHz baseband bandwidth of the 2–1 cascade modulator can be met with NMOS input amplifiers [17],[15]. As a result, the operational amplifier in Figure 4.8 was selected for use in the 2-1 cascade sigma-delta modulator.

4.4 AMPLIFIER DESIGN AND POWER OPTIMIZATION

This section develops design procedures and power-optimization strategies for the operational amplifier topology in Figure 4.8. The approach is to provide design equations which illustrate trade-offs when picking device sizes and bias points with emphasis on minimizing power dissipation and providing robust implementations. Design equations for dc gain, small-signal frequency response, step-response, thermal noise and slew rate are derived. Since the cascode compensation scheme creates an amplifier with three closed-loop poles, the design

equations become significantly more complicated than for a single-stage or conventional Miller compensated two-stage amplifier. This implies that for practical designs some form of computer optimization constrained by the trade-offs illustrated in the design equations will be necessary [11,[17],.

4.4.1 DC GAIN

A small-signal half circuit model which can be used to calculate the amplifier dc gain is shown in Figure 4.9. The model neglects all capacitances which only affect the amplifier frequency response. From small-signal analysis, it can be shown that the dc gain of the amplifier is given by Eq. (4.11). As expected, the gain is on the order of $(g_m r_o)^3$.

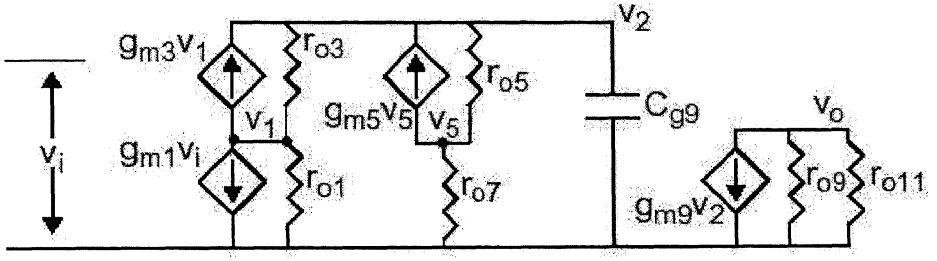


FIGURE 4.9 SMALL SIGNAL MODEL FOR DC GAIN CALCULATIONS

$$A_{dc} = g_{m1}g_{m9}\left[r_{o1}(1+g_{m3}r_{o3}) \| r_{o5}(1+g_{m5}r_{o7})\right](r_{o9} \| r_{o11}) \tag{4.11}$$

The dc gain in Eq. (4.11) provides a starting point for sizing certain devices in the amplifier. To provide adequate margin for process variations and assure that the leak specification is met, it is desirable to maximize the amplifier dc gain. DC gain is maximized when it is limited by the NMOS devices in the signal path. In the first stage of the amplifier, this implies that the output resistance of the PMOS active load should be made much larger than the output resistance of the NMOS input and cascode device as given in Eq. (4.12).

$$r_{o5}(1+g_{m5}r_{o7}) >> r_{o1}(1+g_{m3}r_{o3}) \tag{4.12}$$

Since M_7 and M_8 in Figure 4.8, does not capacitively load the signal path, these devices can be made long channel to maximize r_{o7} in dc gain equation Eq.

(4.11). If this is still not sufficient to satisfy Eq. (4.12), M_5 and M_6, the PMOS cascode devices, in Figure 4.8 can be increased in channel length. Since the output capacitance of these devices loads the output of the first stage of the amplifier, speed and dc gain will trade off through the channel length of the cascode devices. DC gain of the second stage of the amplifier is maximized when it is limited by the NMOS devices M_9 and M_{10} in Figure 4.8. An additional constraint is that the second stage gain needs to be large enough that the first stage devices will remain in saturation for the worst case output swing. Practically, this implies that the PMOS current source loads M_{11} and M_{12} in Figure 4.8 will need to be increased from the minimum channel length. Since the output capacitance of M_{11} and M_{12} directly loads the output of the amplifier, speed and dc gain will also trade off through the channel length of these PMOS devices.

4.4.2 THERMAL NOISE

The input-referred thermal noise of a single common-source transistor, shown in Figure .7 can be approximated by

$$\overline{v_{n,in}^2} \approx \overline{i_{ds}^2} \cdot g_m^{-2} = 4kT\frac{2}{3}\frac{1}{g_m} n_{SC}\Delta f \tag{4.13}$$

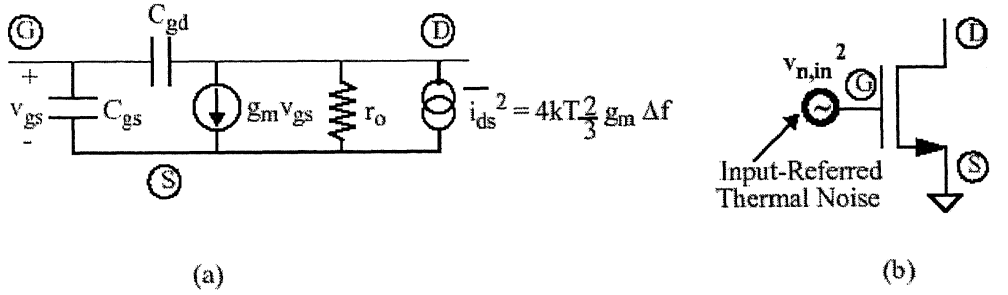


FIGURE 4.10 THERMAL NOISE IN A SINGLE COMMON SOURCE TRANSISTOR (A) SMALL-SIGNAL MODEL (B) INPUT-REFERRED NOISE VOLTAGE

The factor n_{sc} takes into consideration the additional noise in short-channel devices and is bias dependent. The results of Eq. (4.13) can be applied to determine the input referred thermal noise of the OTA. A simple analysis of the small-signal model will show that the noise contribution from the cascode devices

is negligible. Moreover, the noise of the devices in the second stage, when referred to the input of the OTA, is attenuated by the square of the gain of the first stage. As such, the input-referred thermal noise is dominated by the input devices (M_1, M_2) and the load devices (M_7, M_8), as shown below.

$$P_{n,OTA} = 2\left\{ v_{n1,in}^2 + \left(\frac{G_{m3}}{g_{m1}}\right)^2 v_{n3,in}^2 + \left(\frac{G_{m5}}{g_{m1}}\right)^2 v_{n5,in}^2 + \left(\frac{g_{m7}}{g_{m1}}\right)^2 v_{n7,in}^2 + \left(\frac{1}{A_{dc1}}\right)^2 \left[v_{n9,in}^2 + \left(\frac{g_{m11}}{g_{m1}}\right)^2 v_{n11,in}^2 \right] \right\}$$
$$= 2\left\{ 4kT\frac{2}{3}\frac{1}{g_{m1}}\left[1+\frac{g_{m7}}{g_{m1}}\right] \right\}\Delta f \qquad (4.14)$$

When the amplifier is placed in the switched-capacitor integrator, the total noise power is evaluated by integrating the noise spectrum to infinity. This is because the sampling process causes the noise spectrum at high frequencies to fold down to baseband. The Δf term in Eq. (4.14) should therefore be the bandwidth of the integrator. The thermal noise of the OTA, when referred to the output of the integrator, is shown below [16].

$$P_{OTA,out} = \int \left[P_{n,OTA} \frac{1}{f_{FB}^2} \left| \frac{1}{1+\frac{sC_C}{g_{m1}f_{FB}}} \right|^2 \right] df \qquad (4.15)$$
$$\cong \frac{2}{3}\frac{kT}{C_C}\frac{\left(1+\frac{g_{m7}}{g_{m1}}\right)}{f_{FB}}$$

where, $$f_{FB} = \frac{C_F}{C_F + C_S + C_{in}} \qquad (4.16)$$

Eq. (4.15) suggests that decreasing the ratio (g_{m7}/g_{m1}), will minimize the OTA thermal noise. Because the transconductance gm is given by

$$g_m = \frac{2I_{DS}}{V_{DS}^{sat}} \qquad (4.17)$$

it is desirable to minimize of the ratio $V_{DS1}^{sat}/V_{DS7}^{sat}$. In addition, the compensation capacitor needs to be sufficiently large to keep the OTA noise contribution minimal.

4.4.3 FLICKER NOISE

Flicker noise is due to the random trapping and de-trapping of minority carriers in the channel of MOS devices. Because the fluctuations in the channel charge carrier density have a relatively large time constant, the noise power density is inversely proportional to frequency. This is why flicker noise is also commonly referred to as $1/f$ noise. The input-referred flicker noise of a single common-source transistor is given by

$$v_{fl,in} = \frac{K_F}{WLC_{OX}f}\Delta f \tag{4.18}$$

The constant K_F is a fitting parameter which differs from process to process. NMOS devices demonstrate a higher flicker noise characteristic compared to their PMOS counterparts. A straightforward strategy to reduce the flicker noise is to increase gate area, i.e. width and length, of the device. There are circuit techniques at the integrator level which can be employed to provide a first-order cancellation of the $1/f$ noise. Two such techniques are correlated double sampling and chopper stabilization [20]-[23].

For design simplicity, the OTA flicker noise contribution is reduced by increasing the sizes of the input (M_1, M_2) and load (M_7, M_8) devices. By increasing both the width and length by the same factor, the gate area is increased without changing the W/L ratio. For a fixed current, this keeps a constant transconductance (g_m) and saturation voltage V_{DS}^{sat}. Increasing the input device sizes, however, increases the input parasitic capacitances, which in turn degrades the feedback factor. This is tolerable in this system because of the relatively large sampling and integrating capacitors.

4.4.4 LINEAR SETTLING

The OTA needs to have a sufficient bandwidth for the signal to linearly settle to the desired accuracy within half a clock period, as shown below.

$$\omega_{uT} = \frac{1}{\tau} \geq 2 f_S . n_\tau \tag{4.19}$$

The sampling frequency f_S is determined by the signal bandwidth and the required oversampling ratio, and n_τ is the number of time constants.

The frequency response of the amplifier will now be analyzed to provide an understanding of how circuit parameters affect the unity-gain bandwidth.

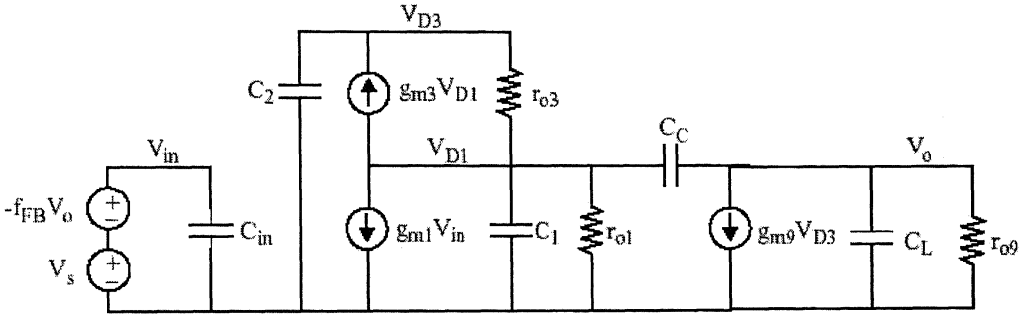


FIGURE 4.11 SMALL-SIGNAL MODEL FOR FREQUENCY RESPONSE CALCULATIONS

Figure 4.11, shows the small–signal model of the amplifier. The capacitors in the figure are defined below.

$$C_{in} = C_{gs1} + C_{P,switch} \tag{4.20}$$

$$C_1 = C_{gd1} + C_{gs3} \tag{4.21}$$

$$C_2 = C_{gd3} + C_{gd5} + C_{gs9} \tag{4.22}$$

$$C_L = C_{gd9} + C_{gd11} + C_I(1 - f_{FB}) + C_{I,bottom} + C_{C,bottom} + C_{next} \tag{4.23}$$

The quantities $C_{I,bottom}$ and $C_{C,bottom}$ are respectively the bottom-plate parasitic capacitances for the integrating and compensation capacitors. $C_{P,switch}$ refers to the parasitic capacitance due to the transfer switch at the summing node, while C_{next} is the parasitic capacitance due to the sampling switches in the next stage.

Assuming infinite device output resistance, r_O, it can be shown that the amplifier transfer function is given by Eq. (4.24) [22],[23].

$$H(s)=\frac{\frac{g_{m1}}{C_2C_T^{\,2}}\left(g_{m3}g_{m9}-C_2C_C s^2\right)}{s^3+\left[\frac{g_{m3}(C_L+C_C)-fg_{m1}C_C}{C_T^{\,2}}\right]s^2+\frac{g_{m3}g_{m9}C_C}{C_2C_T^{\,2}}s+\frac{fg_{m1}g_{m3}g_{m9}}{C_2C_T^{\,2}}} \tag{4.24}$$

where,
$$C_T^{\,2}=C_1C_L+C_1C_C+C_LC_C \tag{4.25}$$

Although Eq. (4.24) provides a complete quantitative solution, it is too complicated for hand calculations. Many simplifying assumptions can be made to allow the designer to approximate the pole locations.

The closed-loop unity-gain bandwidth in Eq. (4.19) can be rewritten in terms of circuit parameters. Since the feedback factor f_{FB} is constant for a fixed gain, and because the

$$\omega_{UT}\approx\frac{g_{m1}}{C_C}f_{FB} \tag{4.26}$$

compensation capacitor C_C is determined by thermal noise considerations, the minimum transconductance of the input devices g_{m1} can be calculated from Eq. (4.19) and Eq. (4.26).

The two open-loop non-dominant poles can be approximated by

$$|p_2|\approx\frac{g_{m9}}{C_F(1-f_{FB})+C_{gd11}+C_L} \tag{4.27}$$

$$|p_3|\approx\frac{g_{m3}}{C_C+C_{gs3}+C_{gd1}+C_{sb3}} \tag{4.28}$$

For the amplifier to remain stable, the non-dominant poles should be made much larger than the unity-gain bandwidth. From Eq. (4.26) and Eq. (4.27), it is obvious that

$$g_{m9}>>g_{m1}f_{FB}\frac{C_F(1-f_{FB})}{C_C} \tag{4.29}$$

From Eq. (4.26) and Eq. (4.28), the transconductance of the NMOS cascode devices (M_3, M_4) should be made larger than the transconductance of the input devices (M_1, M_2).

$$g_{m3} >> g_{m1} f_{FB} \tag{4.30}$$

4.4.5 SLEW RATE

When a large input step is applied to the amplifier, its output is unable to track the large rate of change in its input. This is due to the limit in the differential current which the class A amplifier can deliver. This nonlinear response is known as the amplifier's slew rate. The amplifier may approach a slew limit in either the first or second stage. The slew limit in the first stage is determined by the need to charge the compensation capacitor at the source of M_3 and M_4, while the slew limit in the second stage is set by the need to charge the load and compensation capacitors. This suggests that for a fixed settling specification, the slew rate can be improved by increasing the V_{GS}–V_{TH} of the input devices (M_1, M_2, M_9 and M_{10}). This requires increasing bias current, as suggested by Eq. (4.31).

$$SR = \min\left(\frac{2I_1}{C_C}, \frac{2I_9}{C_C + C_L}\right) \tag{4.31}$$

4.5 COMMON-MODE FEEDBACK

Common-mode feedback is required in fully-differential amplifiers to define the voltages at the high-impedance output nodes. The amplifier employs dynamic or switched–capacitor common-mode feedback. The fully-differential second stage eliminates the need for an inversion stage in the common-mode feedback loop. Figure 4.12 shows the common-mode feedback loop for the first stage of the amplifier. Capacitors C_M are used to sense the output common-mode voltage. During Φ_{2d}, switched capacitors C_{CM} define the appropriate DC voltage on the sense capacitors. The loop works by steering current from current source M_{13cm}. The total tail current source has been split into M_{13} and M_{13cm} for improved stability. A similar loop is designed for the second stage of the amplifier.

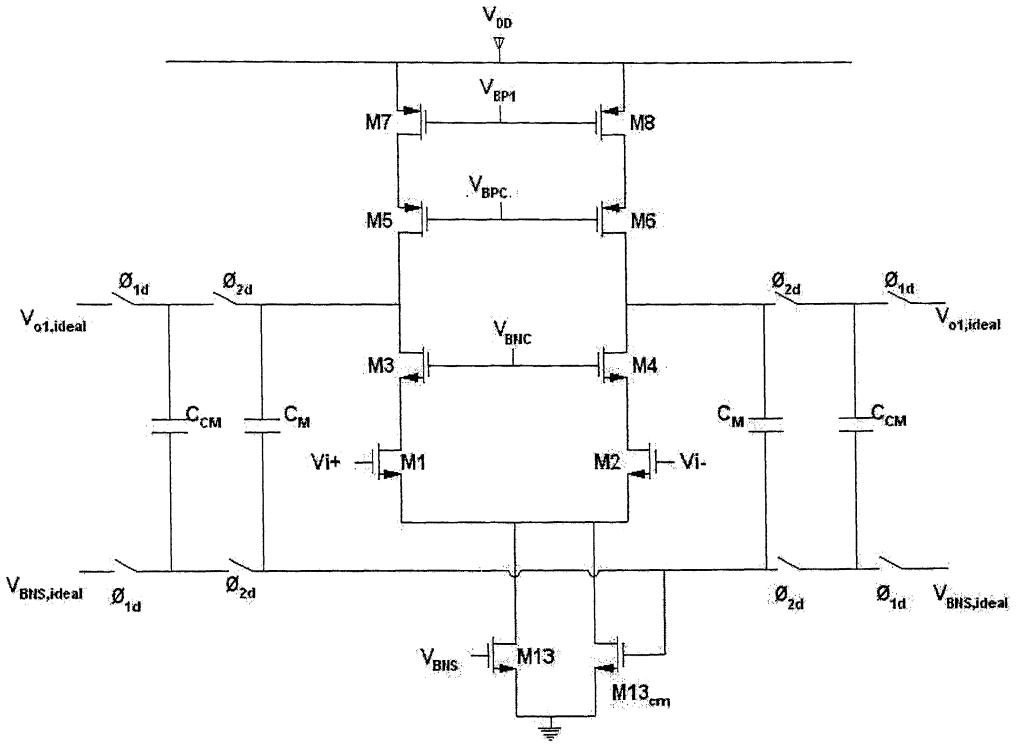


FIGURE 4.12 COMMON-MODE FEEDBACK IN THE 1ST STAGE OF OTA

4.6 BIAS

Figure 4.13 shows the biasing network for the OTA. One master current source is used and a variety of bias currents are generated using current mirrors. High-swing biasing is adopted for both PMOS and NMOS cascode devices, and an internal cascode bias is used for M_3 and M_4 as shown in Figure 4.14. The V_D^{sat}'s of the biasing devices are chosen to be identical to those in the OTA to ensure good matching. Devices M_{7b} and M_{11b} are also made longer (same asM_7—M_8 and M_{11}—M_{12}, respectively) to improve matching. In addition, the V_{DS} of the amplifier transistors are biased to be 100mV greater than their respective V_D^{sat}'s. Decoupling capacitors to V_{DD} (PMOS bias) or ground (NMOS bias) are used at all biasing nodes to keep the DC bias voltages stable. Power dissipation can be reduced by decreasing the currents in the biasing stage. The biasing currents are chosen to be approximately one tenth (0.1) of the currents in the amplifier. To provide good

4.7 COMPARATOR

A simple dynamic comparator is shown in Figure 4.15 [10],[11], is used to perform a single–bit conversion. During phase 2, when the latch signal is low, the differential outputs are reset to V_{DD}. As the latch signal turns high, the differential inputs control the resistance of the triode devices, M_1 and M_2. Based on this differential resistance, the outputs of the cross-coupled inverters (M_3, M_4, M_7 and M_8) flip in the appropriate direction. Power dissipation is minimized by using the dynamic comparator shown in Figure 4.15.

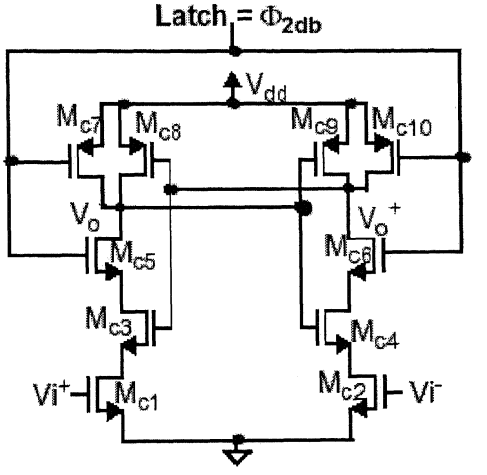


FIGURE 4.15 DYNAMIC COMPARATOR

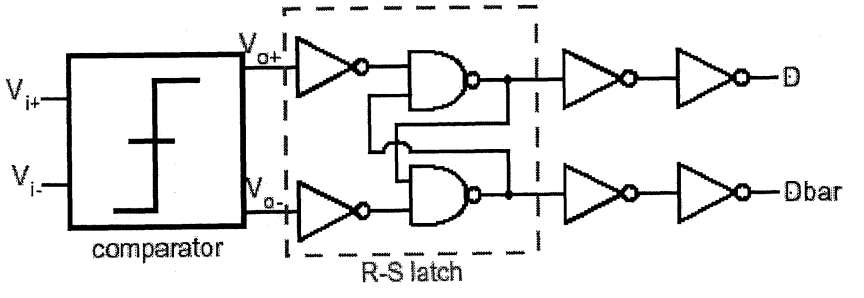


FIGURE 4.16 COMPARATOR WITH RS LATCH

The fast, regenerative nature of the dynamic comparator, coupled with the memory inherent to the RS latch, reduces the possibility of metastability to very low

levels. Instead, if the comparator is unable to resolve the input signal in the allotted time, the RS latch holds its previous state. Hence, metastability is converted to hysteresis.

4.8 TWO-PHASE CLOCK GENERATOR

As discussed in Section 4.2, the integrators need a 2-phase non-overlapping clock (with delays) to minimize signal-dependent charge-injection errors. Figure 4.17 shows the waveform of the 2-phase clock. Φ_{1d} and Φ_{2d} are the delayed versions of Φ_1 and Φ_2. The rising edges of the delayed clocks should be lined up with the rising edges of the non-delayed versions to increase the amount of available settling time for the OTA, which is given by

$$t_{settle} = \frac{T_S}{2} - t_{nol} - t_r - t_f$$

where, T_S is the sampling period, t_{nol} is the non-overlap time, t_r and t_f are raise and fall times, respectively.

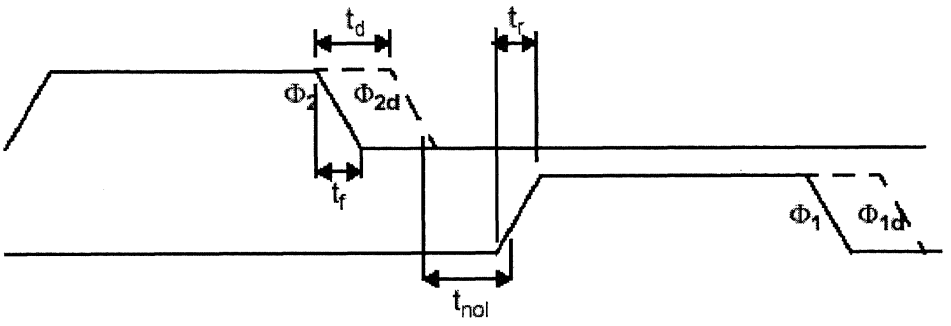


FIGURE 4.17 TIMING WAVEFORM OF TWO-PHASE NON-OVERLAP CLOCKS

The circuit formed by M_1-M_3 and M_4-M_6 in Figure 4.18 line up the rising edges of the delayed and non-delayed clocks. The delay and non-overlap times are affected by the delays in the inverter chain and the NAND gates.

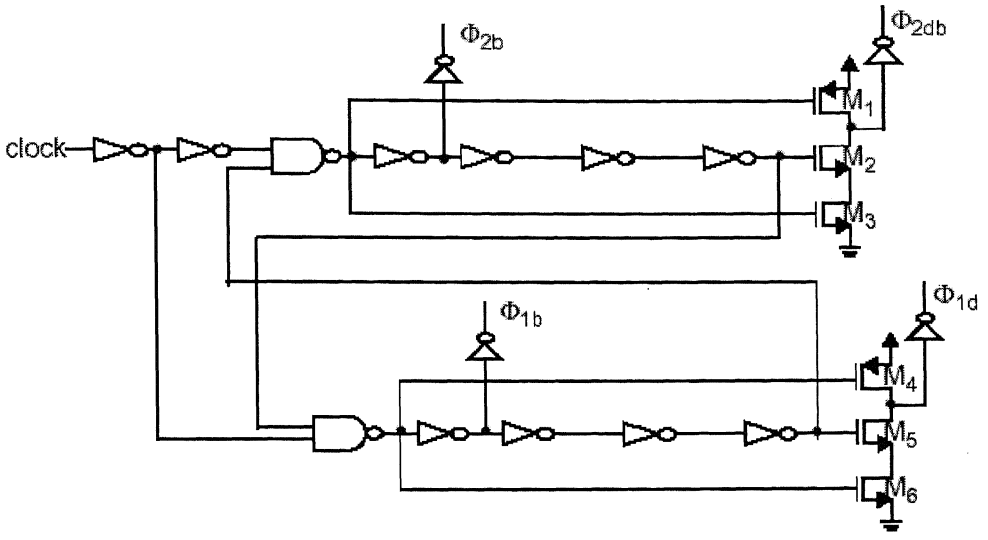


FIGURE 4.18 TWO-PHASE CLOCK GENERATOR

4.9 SUMMARY

This chapter presented fundamental issues and tradeoffs in the design of the key circuit blocks: integrators, amplifiers, comparators, 2-phase clock generators, and output buffers. Power optimization techniques for the operational transconductance amplifier were investigated.

Chapter 5

SIMULATED RESULTS

5.1 INTRODUCTION

This chapter discusses the behavioral level and transistor level simulation results of a 2-1 cascaded (MASH) ΣΔ modulator. Transistor level simulations are done using TSMC 0.25μm CMOS technology [26]. The discussion will begin with the behavioral level simulation results and the effect of non idealities on the modulator using Matlab, SIMULINK. In the next section, transistor level simulation design of various circuit blocks is discussed and the simulated results of the cascaded architecture are presented. Tanner tools are used for transistor level simulations.

5.2 BEHAVIORAL LEVEL SIMULATION RESULTS

5.2.1 IDEAL MODULATOR

As discussed in section 3.2, the ideal 2-1 cascaded ΣΔ modulator is designed in Matlab Simulink. The Simulink model of the block diagram discussed in Figure 3.2 is shown in Figure 5.1 [27].

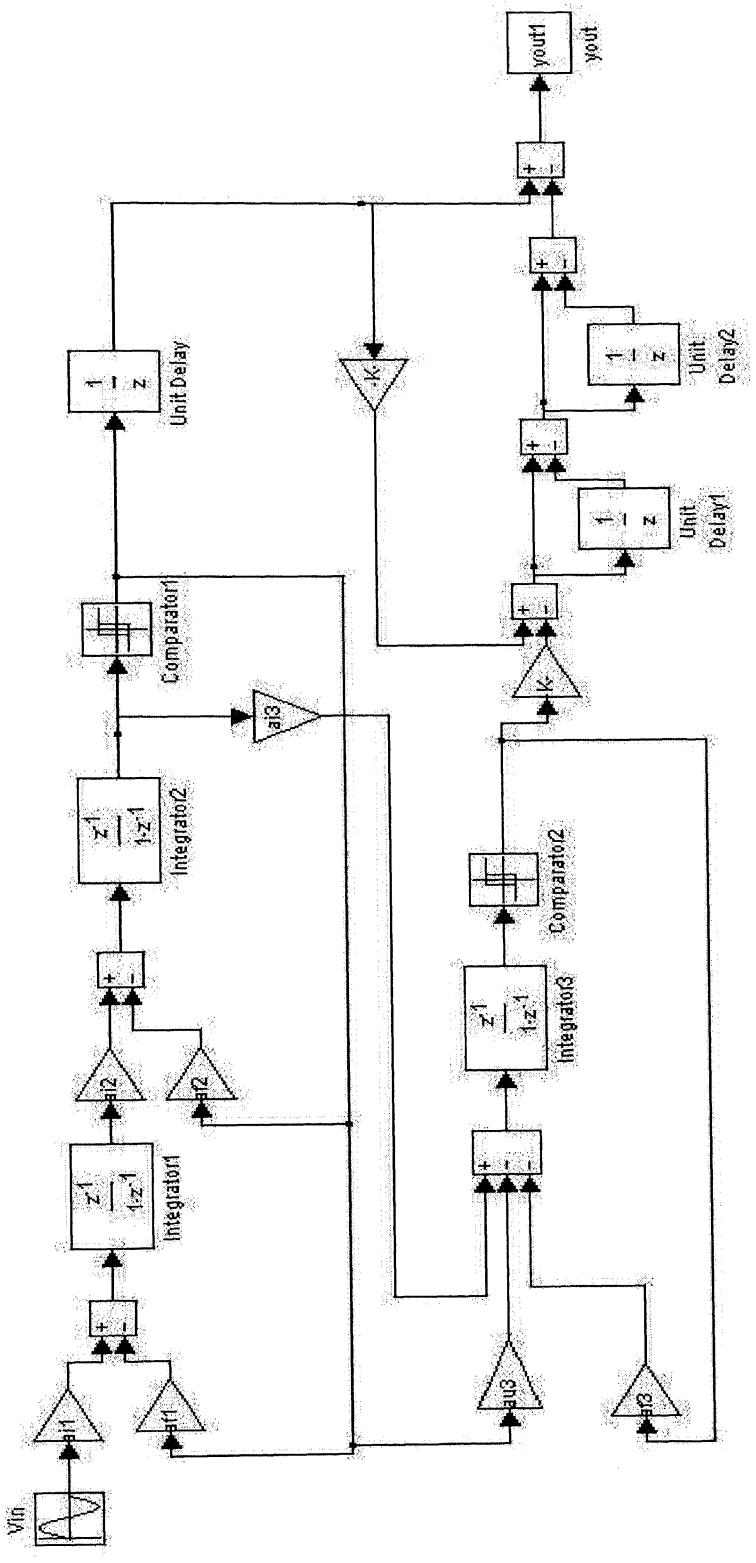


FIGURE 5.1 IDEAL 2-1 CASCADED (MASH) ΣΔ MODULATOR

Sampling frequency (f_S) used for simulations is 20.48 MHz, i.e, oversampling ratio (OSR) is 64. The integrators gains used in this design are summarized in Table 5.1 [4],[5],[15].

Gain	a_{i1}	a_{f1}	a_{i2}	a_{f2}	a_{u3}	a_{i3}	a_{f3}
Value	1.0	0.2	0.5	0.25	0.5	0.1	0.1

TABLE 5.1
INTEGRATOR GAIN VALUES

The peak SNR obtained for the ideal modulator is 102.4 dB at 6 dB input signal amplitude. SNR versus Signal amplitude for the above model is shown in Figure 5... The test input signal used for our simulations is 300 mV of sinusoidal signal at the frequency of 50 KHz. Figure 5.2 shows the 65536 (64K) FFT of the output spectrum for the test input signal. The SNR obtained is 92.8 dB, i.e. 15.13 bits of resolution (from Eq. (2.11)).

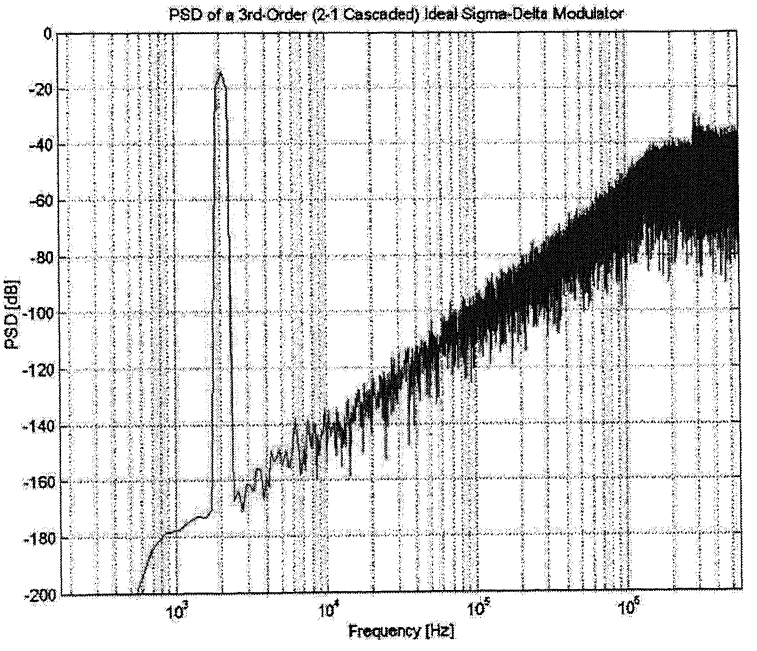


FIGURE 5.2 OUTPUT SPECTRUM FOR IDEAL 2-1 CASCADED ΣΔ MODULATOR

From the Figure 5.2, it clearly shows that the quantization noise tones are shifted to higher frequencies which are not in the required band of range. Hence, the modulator achieves a high SNR by sampling the input signal with a higher rate.

5.2.2 NON IDEAL MODULATOR

The ideal modulator doesn't consider the nonidealities of the modulator, which greatly affects the performance of the modulator. Before going for transistor level simulations, we should know the behavior of the modulator for nonideal building blocks. The Simulink model for 2-1 cascaded (MASH) architecture is shown in Figure 5.3 which includes all the nonidealities that are discussed in sections 3.3 and 3.4 [12][15].

The design parameters used for the behavioral level nonideal simulations are summarized in Table 5.2.

Parameter	Value
Signal Bandwidth	320KHz
Sampling Frequency	20.48MHz
Oversampling Ratio	64
Number of samples Considered	65536

TABLE 5.2
PARAMETERS OF THE 2–1 CASCADED ΣΔ MODULATOR

In the circuit shown in Figure 5.3, only the non idealities of the first integrator are considered, since their effects are not attenuated by the noise shaping. To estimate the performance of the modulator, we varied the values of the nonideal parameters that are used in simulations and calculated the corresponding SNR.

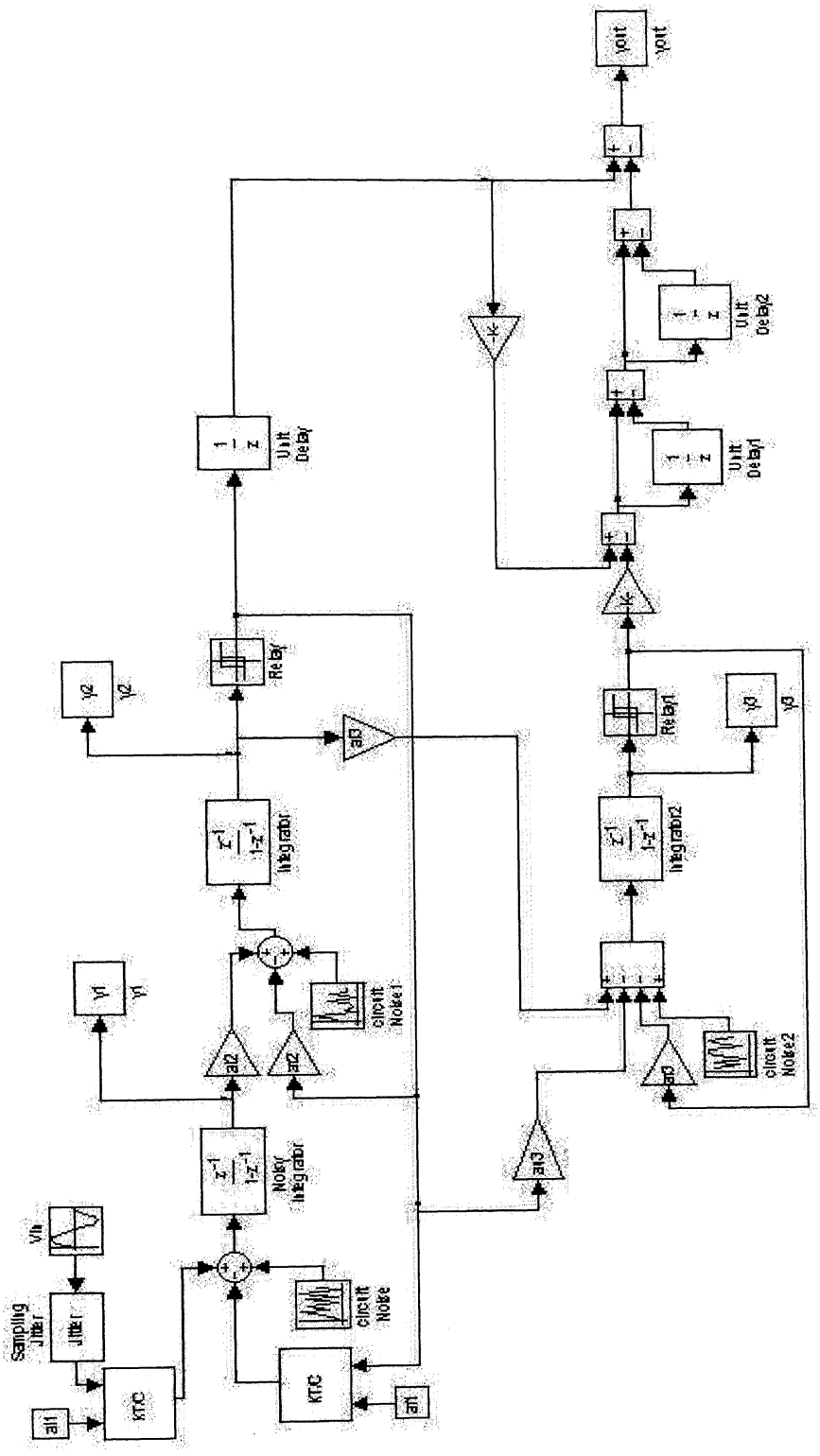


FIGURE 5.3 NON–IDEAL 2-1 CASCADED (MASH) ΣΔ MODULATOR

The main nonideal parameter that affects more on SNR of the modulator is finite DC gain of the first integrator. These effects are shown in the Figures 5.4–5.5. Figure 5.4 shows the plot of SNR and the finite DC gain of the amplifier for different oversampling ratios. The plot doesn't consider the effect of other nonideal parameters. Figure 5.5 shows the plot of SNR and finite DC gain for the oversampling ratio of 64 considering the other non-ideal parameters. From the plot, it is easily shown that, as the gain decreases the SNR also decreases as explained in section 3.3. The gain required for the OTA of the first integrator is obtained from this figure, i.e. the gain should be greater than 65 dB.

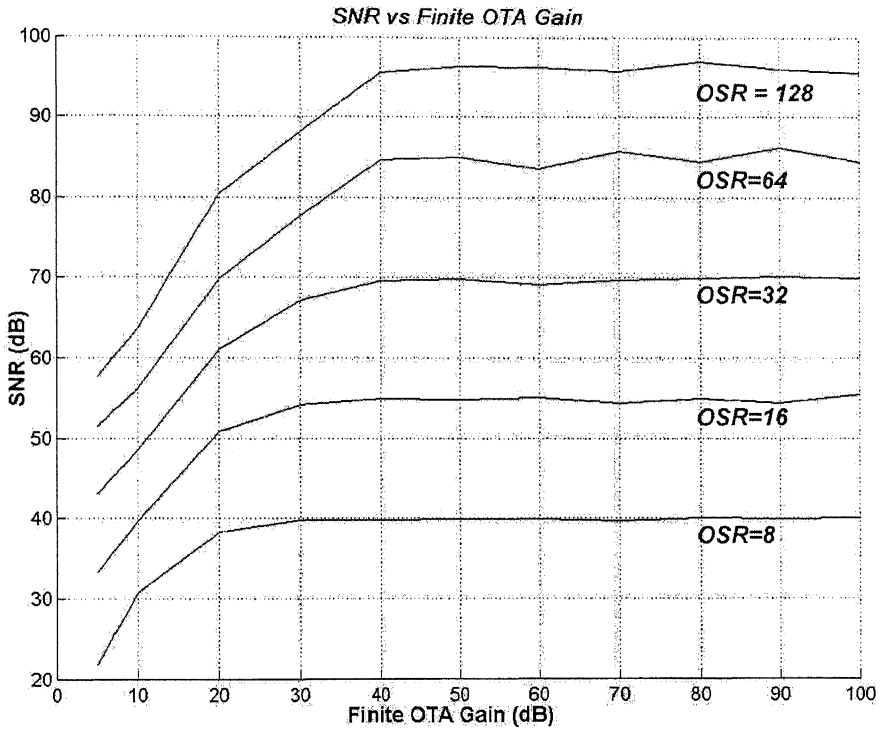


FIGURE 5.4 SNR VERSUS OTA GAIN FOR DIFFERENT OSR'S

Table 5.3 shows the results obtained from the behavioral level simulations for the transistor level designing.

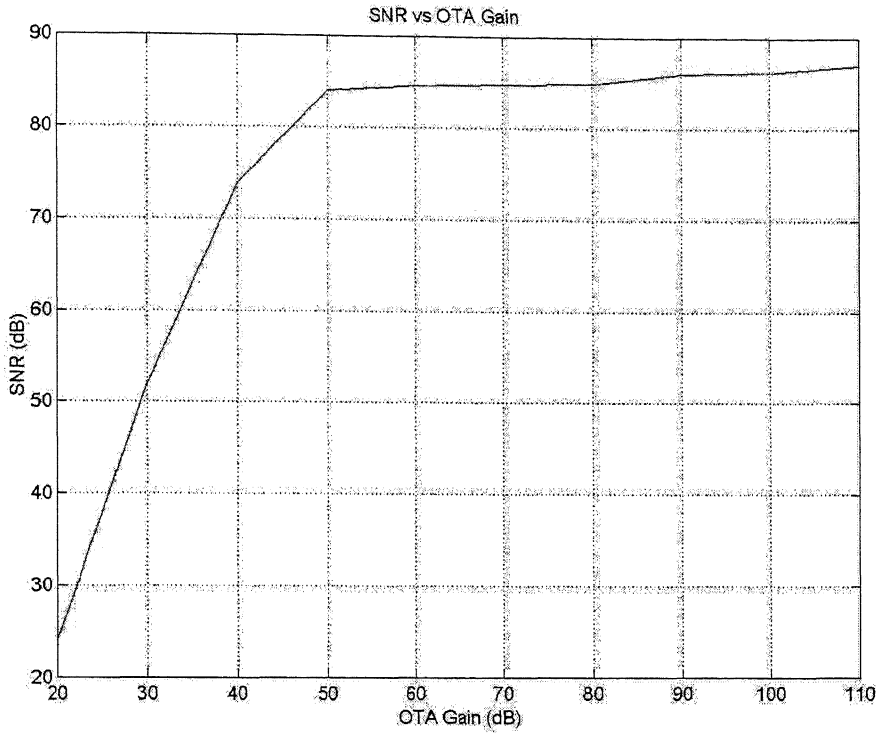


FIGURE 5.5 SNR VS OTA GAIN FOR OSR = 64, CONSIDERING OTHER NON-IDEAL PARAMETERS

Modulator Non-ideal Parameter	Value
Sampling Jitter	10 nS
Switches (KT/C_S) Noise	1.5 pF
Parasitic Capacitance of OTA (C_P)	300fF
Input referred Op-Amp thermal noise	20 μV_{rms}
Finite Op-Amp DC gain	70 dB
Gain Bandwidth Product of Op-Amp	175 MHz
Slew Rate	210 V/μS

TABLE 5.3 MODULATOR NONIDEALITIES

For the test input signal, i.e. 300 mV, 50 KHz sinusoidal input signal, output spectrum of 65536 FFT is shown in Figure 5.6. The SNR obtained for the test input signal is 86.5 dB, i.e. resolution of 14.1 bits.

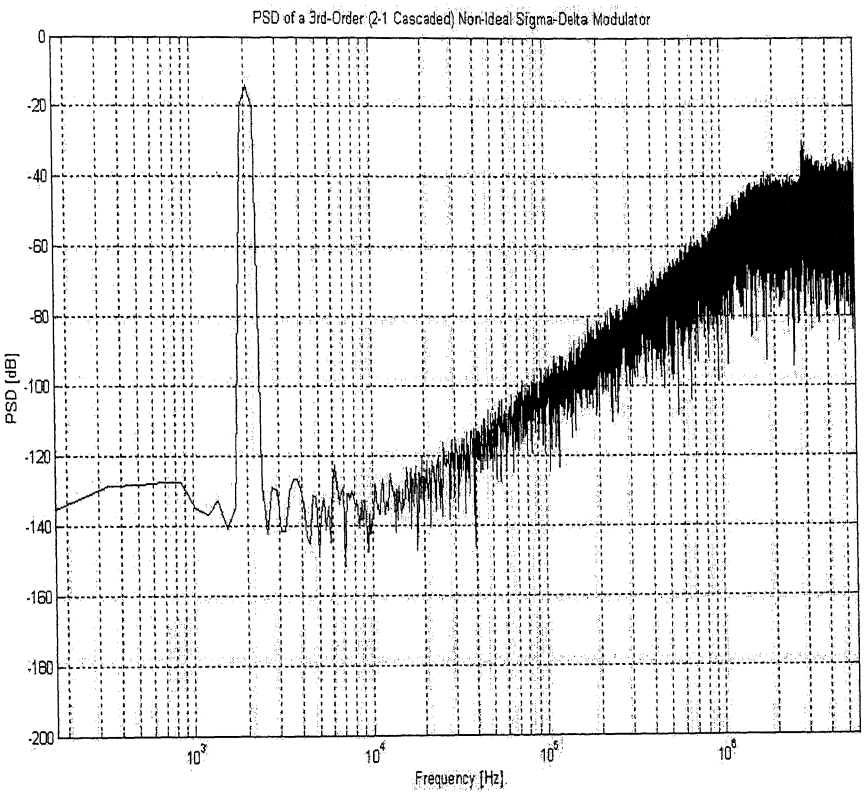


FIGURE 5.6 OUTPUT SPECTRUM FOR NON-IDEAL BEHAVIORAL MODEL

Comparing the ideal modulator and nonideal modulator output spectrums, it is clear that all there are some noise tones present in the required band of frequencies. This is due to the nonidealities of building blocks as explained in Chapter 3.

Figure 5.7 shows the plot of the SNR versus input signal amplitude of both ideal and nonideal cascaded 2-1 ΣΔ modulator. The peak SNR obtained for the nonideal behavioral level simulation is 92.8 dB at 8.5 dB signal amplitude. The dynamic range obtained in ideal and nonideal simulations are 96 dB and 84 dB respectively.

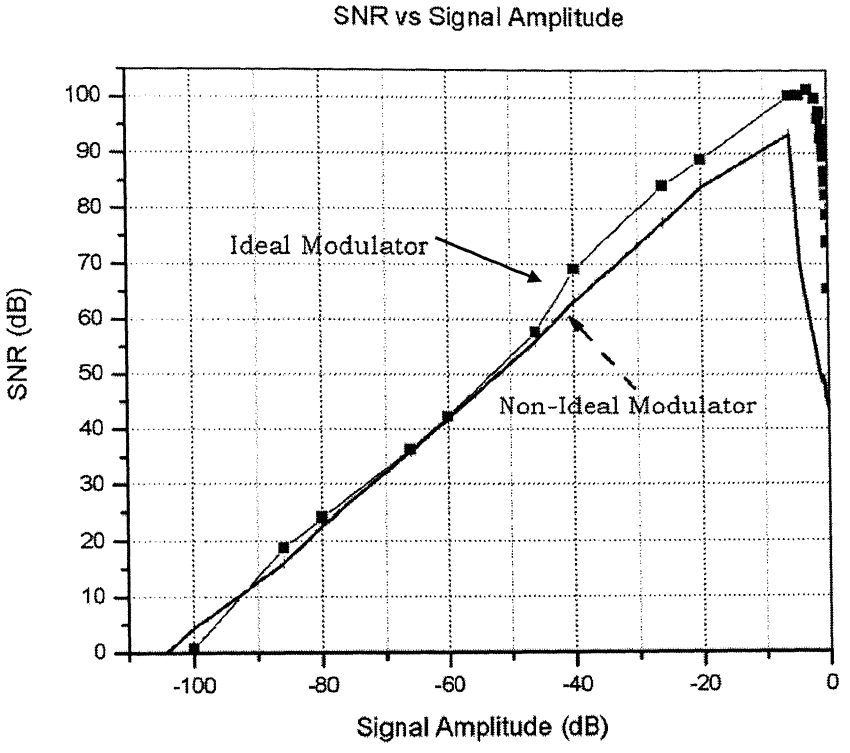


FIGURE 5.7 SNR VS INPUT SIGNAL AMPLITUDE FOR IDEAL AND NON-IDEAL MODULATORS

5.3 TRANSISTOR LEVEL SIMULATION

This section will present the values selected for the capacitors and current levels in the integrators. From the behavioral level simulations, we are able to find out the minimum requirements for designing the first stage integrator. The design constraints used for the design are shown in Table 5.3. The tradeoffs and optimization for the design of the integrators and amplifiers were discussed in Chapter 4.

All simulations are done using TSMC 0.25 μm CMOS technology [26]. The capacitor values for the second integrator are selected on the basis of thermal noise requirements. The noise contribution of the last integrator are negligible, the capacitor values are parasitic limited. Table 5.4 summarizes the values of sampling and integrating capacitors used in this design. The bias currents in the operational

transconductance amplifier are determined by settling constraints, slew rate considerations and required thermal noise floor [11][13][21][29].

	Sampling Capacitor	Integrating Capacitor
Integrator 1	C_{S1}=1.5pF C_{11}=0.3pF	C_{F1}=1.5pF
Integrator 2	C_{S2}=1pF C_{12}=0.5pF	C_{F2}=2pF
Integrator 3	C_{S3}=0.25pF C_{21}=1pF	C_{F3}=2.5pF

TABLE 5.4 SUMMARY OF SAMPLING AND INTEGRATING CAPACITOR VALUES

The 2-stage OTA used in this design was shown in Section 4.4, and is repeated here in Figure 5.8.

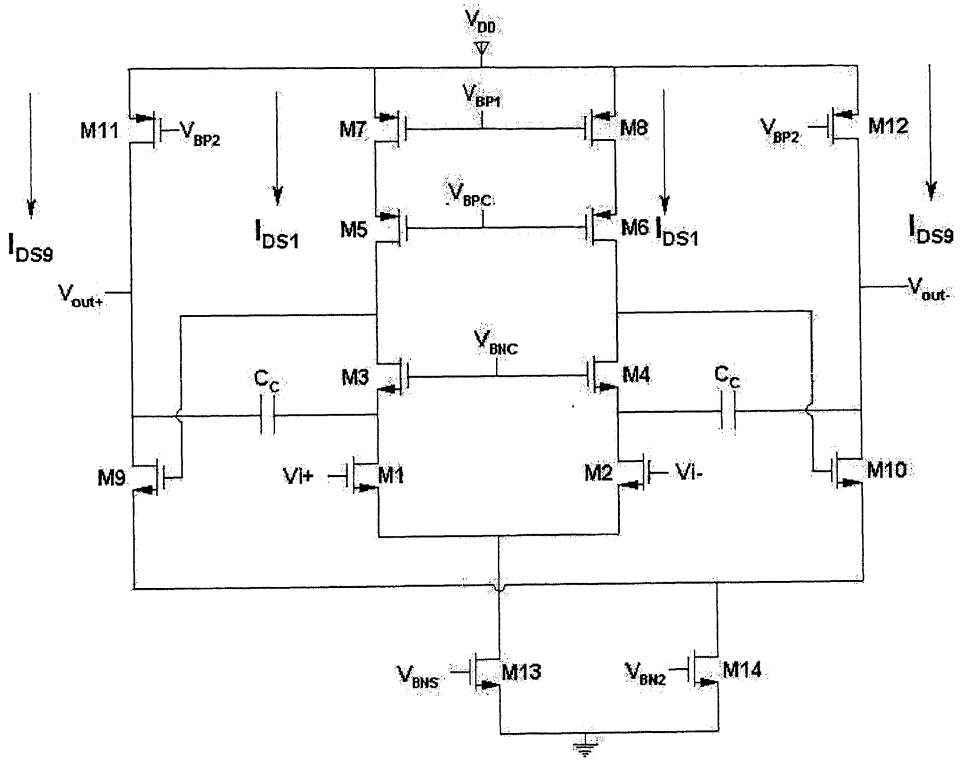


FIGURE 5.8 FULLY DIFFERENTIAL TELESCOPIC CASCADED OTA

Table 5.5 summarizes the settling and slew rate requirements of the three amplifiers in the modulator cascade, and presents the selected values of the bias currents and compensation capacitors.

	Settling Accuracy	Gain (dB)	I_{DS1} (μA)	I_{DS9} (μA)	C_C	GBW (MHz)
Integrator 1	0.04% in 40 ns	78	125	140	2pF	200
Integrator 2	1.5% in 52ns	69	90	110	1pF	145
Integrator 3	2.4% in 56ns	66	80	100	750fF	130

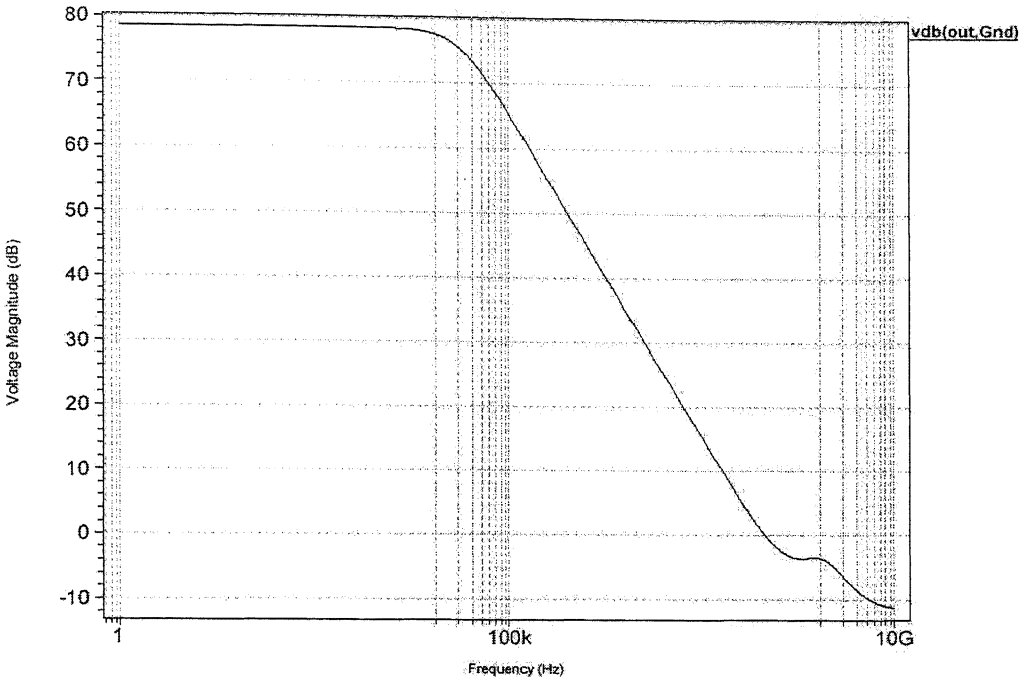
TABLE 5.5 SUMMARY OF BIAS CURRENT'S AND COMPENSATION CAPACITORS IN OTA'S

The value of V_D^{SAT}'s of different transistors affects the input referred noise and the frequency response of the amplifier. Table 5.6 shows the different V_D^{SAT}'s of the OTA and the sizes of the transistors, used in the first stage of integration.

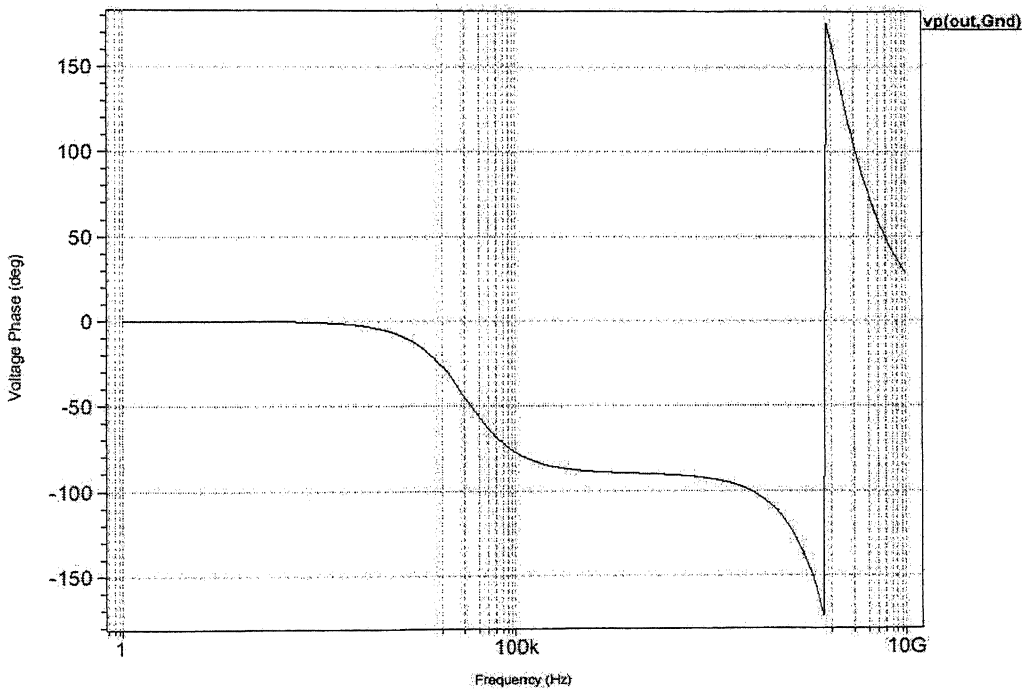
	V_D^{SAT} *(V)*	Size *(μm/μm)*	I_{DS} *(μA)*
M_1, M_2	0.25	11/1	125
M_3, M_4	0.1	24.525/0.25	125
M_5, M_6	0.2	30/0.25	125
M_7, M_8	0.7	8.5/1	125
M_9, M_{10}	0.3	5/0.25	140
M_{11}, M_{12}	0.3	12.5/0.25	140
M_{13}	0.1	39.5/0.25	200
M_{13CM}	0.1	11.25/0.25	50
M_{14}	0.1	51.5/0.25	220
M_{14CM}	0.1	12.75/0.25	60

TABLE 5.6 SUMMARY OF V_D^{SAT}'S AND TRANSISTOR SIZES OF OTA

Figure 5.9 shows the gain plot and the phase margin of the OTA given in Figure 5.8. As discussed in Chapter 3 and section 5.2, the gain of the OTA should be greater than 70 dB. In our design we obtained a gain of 78 dB with a phase margin of 63°. Figure 5.10 shows the slewing action of the OTA, where the slew rate obtained is 22 V/μs. Figure 5.11 shows the output swing of the fully differential OTA. The swing obtained in out design is 5 V pp.



(a)



(b)

FIGURE 5.9 GAIN AND PHASE PLOT OF OTA

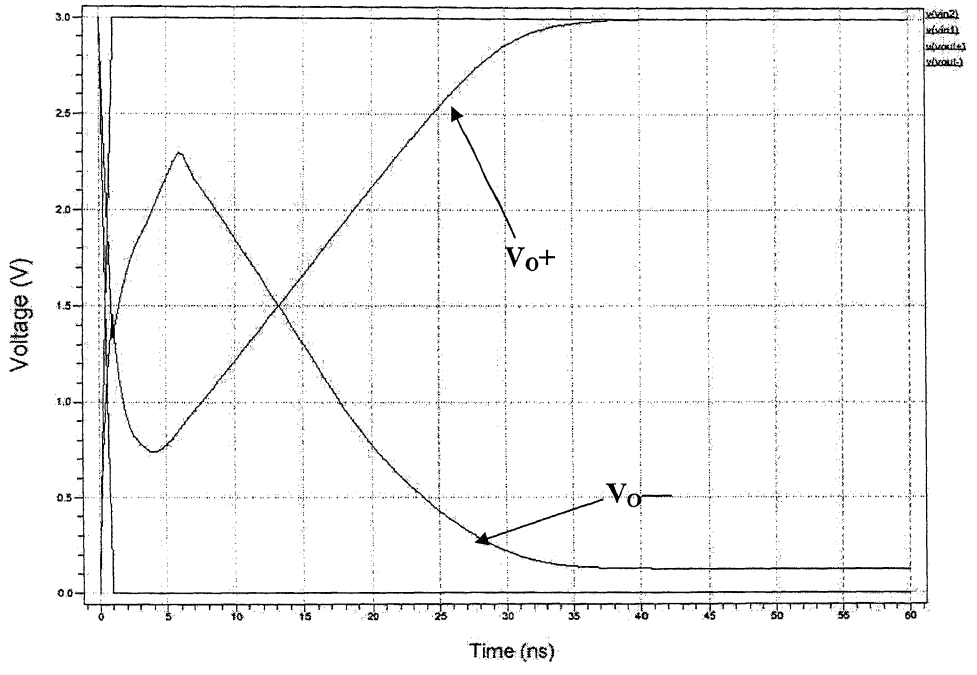


FIGURE 5.10 OUTPUT VOLTAGE FOR A STEP INPUT

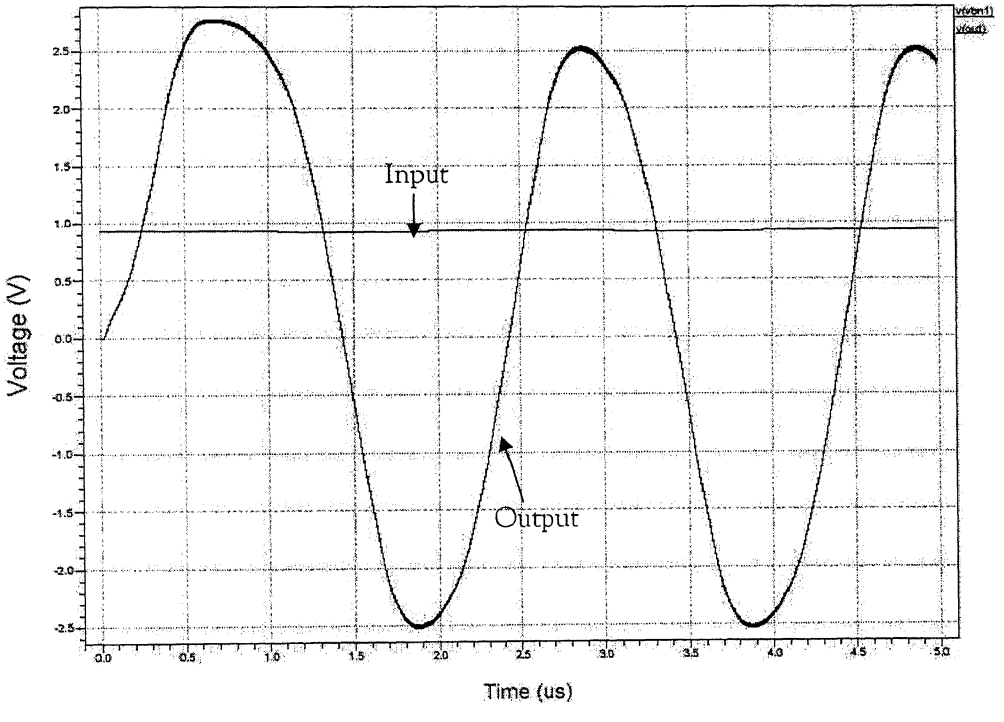


FIGURE 5.11 OUTPUT SWING OF THE OTA

The total design of the third order sigma delta modulator is shown in Figure 5.12. In this figure, the switches are designed using NMOS.

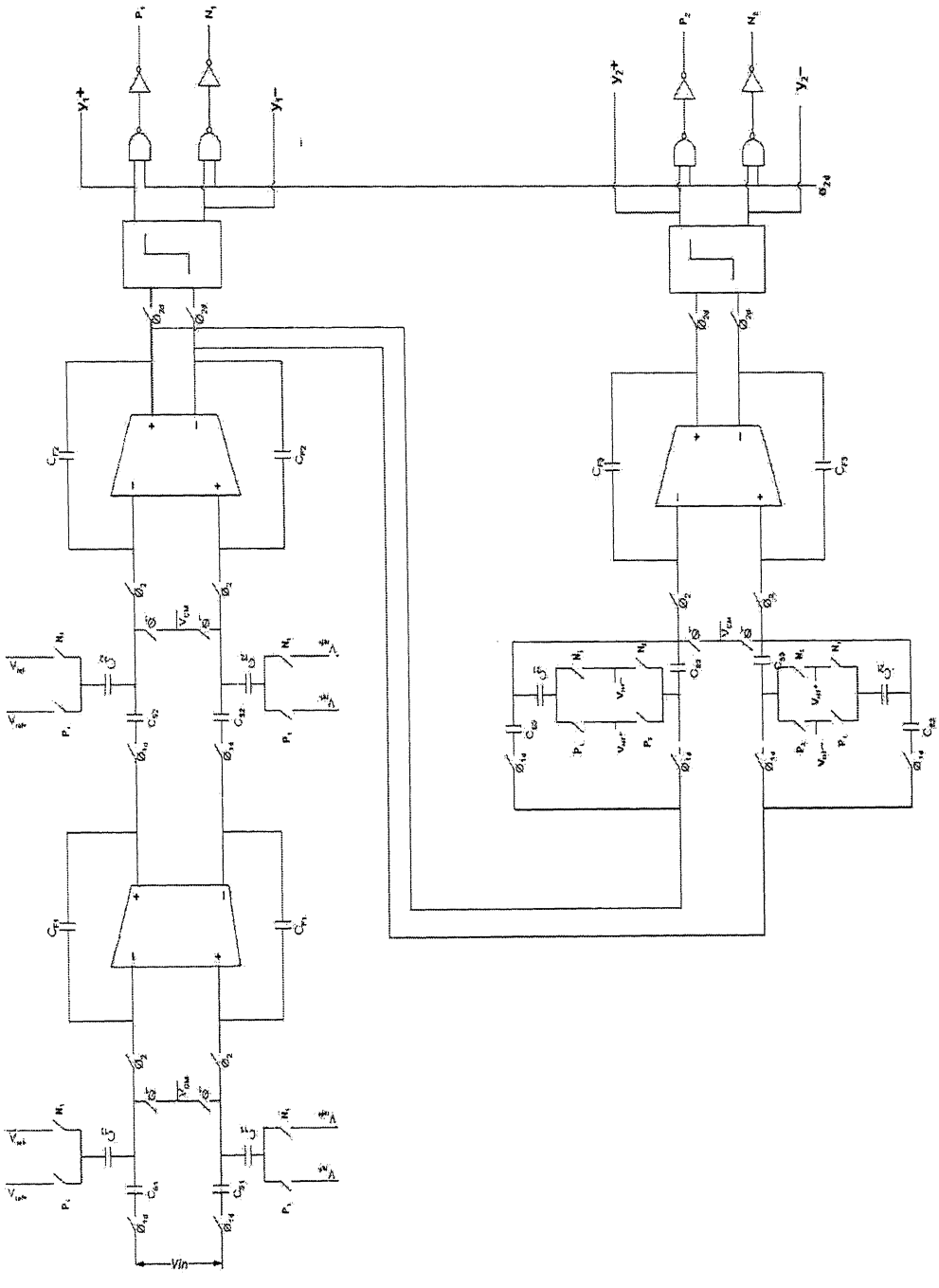


FIGURE 5.12 BLOCK DIAGRAM OF A 2-1 CASCADED (MASH) ΣΔ MODULATOR

All blocks in the Figure 5.12 are designed as discussed in Chapter 4. In the above figure, the comparator outputs are sampled with the clock Φ_{2D}. These outputs (P_1, N_1, P_2 and N_2) are used to give the feedback to the SC integrators. The values of the capacitors used for sampling are mentioned in Table 5.4. The reference voltages used for the feedback (V_{REF+} and V_{REF-}) is ±150 mV. The power dissipation of our design is 90mW. All the simulations are done using Tanner tools (S-Edit for Schematic editing and TSPICE for SPICE level simulations)

The outputs of the first stage and the second stage of the cascaded architecture are to be filtered properly to minimize the quantization noise. As explained in Section 2.6, the digital filters $H_1(z)$ and $H_2(z)$ are to designed precisely to reduce the noise terms at the output, which is described in Eq. (2.21). Here we designed this error cancellation logic using Matlab, Simulink. The cancellation logic used in behavioral modeling is used for this design. The outputs are given to the Matlab program where the digital error cancellation logic is done. Here we had taken the output at the end of clock Φ_{2D}. To calculate the SNR, the outputs of the error cancellation logic are given to the Hamming window and to a 65536 FFT (Appendix C).

When the test input signal of 300 mV, 50 KHz are given, and the corresponding 64K FFT output spectrum after the digital processing is shown in Figure 5.13. The SNR obtained from our design is 83.57 dB, i.e. 13.9 bits of resolution. From Figure 5.13, it is clear that the noise spectrum is spread to the higher frequencies. When compare to the output spectrum of the behavioral level model in Figure 5.6, it is clear that more noise tones are present in the desired frequency range. This is due to the flicker noise and other nonidealities that are not taken in to consideration in behavioral modeling. Table 5.7 shows the SNR and bits resolution for an ideal, nonideal behavior models and transistor level model of 2-1 cascaded ΣΔ modulator, for the test input signal.

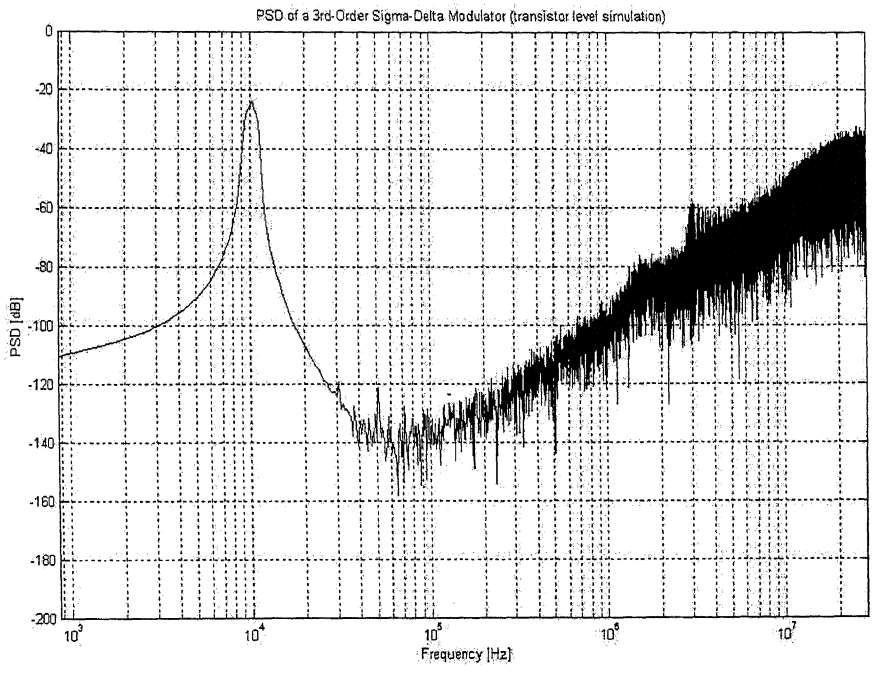


FIGURE 5.13 OUTPUT SPECTRUM FROM TRANSISTOR LEVEL SIMULATION

	Ideal Behavioral Level Simulations	Nonideal Behavioral Level simulations	Transistor Level simulations
SNR (dB)	92.8	86.5	83.57
Resolution in number of bits	15.13	14.1	13.91

TABLE 5.7 SUMMARY OF SIMULATION RESULTS FOR 2-1 CASCADED ΣΔ MODULATOR

5.4 SUMMARY

This chapter present the simulation results of a third order (2–1) cascaded ΣΔ modulator. From the simulation results of non–ideal modulator, we are able to predict the response of the modulator closer to the transistor level simulations. Building blocks are designed using 0.25μm CMOS. The modulator operated at an oversampling rate of 64 and dissipates a power of 90mW from a 3V supply. The modulator achieved 83.57 dB of SNR at 20.48 MHz.

Chapter 6

CONCLUSIONS

6.1 INTRODUCTION

This chapter summarizes the primary research contributions and results, and provides some suggestions for future areas of research. A 2-1 cascaded (MASH) ΣΔ modulator was designed using 0.25μm CMOS process. System-level design of the modulator was presented in Chapter 3, and the design of key circuit blocks was discussed in Chapter 4. Chapter 5 presented the behavioral level and transistor level simulated results.

6.2 SUMMARY OF RESEARCH RESULTS

The research explored design issues of a high-speed switched capacitor ΣΔ modulator for digital audio applications. Emphasis was placed on the low-power design techniques that are amenable to highly integrated analog receivers. A secondary goal was to model the ΣΔ modulators with nonidealities in the system

level for estimating its performance. Key results of this project are summarized below:

- Developed a model implemented in the Matlab, Simulink, environment suitable for time domain behavioral simulations of SC ΣΔ modulators. This model takes accounts most of the SC ΣΔ modulator nonidealities, such as sampling jitter, Thermal noise, switching nonidealities and operational amplifier parameters (white noise, finite DC gain, finite BW, slew rate and saturation voltage).
- Designed a high speed, low power fully differential operational transconductance amplifier suitable for single 3V CMOS processes.
- Designed a SC, CMOS ΣΔ modulator and demonstrated that this circuit would meet the specifications of digital audio applications at reasonable power dissipation. Transistor level simulations achieve an 83.57 dB of SNR at a Nyquist rate of 320 KHz and dissipated 90mW at an oversampling rate of 64.

6.3 FUTURE WORK

This project primarily aims to demonstrate the behavioral level modeling will estimates the performance of real ΣΔ modulator and it is shown using transistor level simulations.

This model can be extended to higher order modulators. This model doesn't consider the flicker noise and nonlinear gain of the OTA. This makes limits on the use of OTA's and the frequency range of the OTA's.

The designed ΣΔ modulator can be extended to higher frequencies that are useful for CDMA and wireless applications.

One area which will be of interest is power-reduction strategies for the high dynamic range baseband circuits. The power dissipation of this circuit can be further reduced by making low power OTA's with charge pumps and also noise due to OTA can be further reduced. Supply voltage scaling can be done to minimize the power and make it use for portable devices.

Another possible future work is to investigate the feasibility of making the modulator adaptable to a very wideband standard like spread-spectrum CDMA and W-CDMA without excessive power dissipation. Achieving 8-10 bits of resolution with a Nyquist rate of 10MS/s or greater involves a somewhat different set of design tradeoffs and optimization than those for this design.

Technology scaling will continue to enable faster ADC's, but new circuit techniques will be necessary if very high speed, high dynamic range ΣΔ modulators are desired. Continuous time ΣΔ (CTΣΔ) modulators have demonstrated the potential to operate at significantly faster sampling rates that discrete-time, SC implementations. Still limited understanding of the design methodologies for CTΣΔ modulators have curbed the design of higher order, multi bit CTΣΔ's. Further research in this area has the potential to allow high dynamic range CMOS ΣΔ modulators with Nyquist rates in the several tens of MHz range.

Multi–bit cascaded ΣΔ modulators can be used to achieve more SNR for lesser oversampling ratios. Further research in this area has the potential to get higher resolution (greater than 18 bits) with out going for higher order ΣΔ modulators.

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Appendix A

SPICE PARAMETERS

MOSIS PARAMETRIC TEST RESULTS

RUN: T33W (MM_NON-EPI) VENDOR: TSMC
TECHNOLOGY: SCN025 FEATURE SIZE: 0.25 microns

T33W SPICE BSIM3 VERSION 3.1 PARAMETERS

*SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

Temperature_parameters=Default

BSIM3 SPICE MODEL FOR NMOS

```
.MODEL      NMOS      NMOS (
+VERSION= 3.1      LEVEL=49      TNOM=27      TOX =5.6E-9
+XJ=1E-7      NCH =2.3549E17      VTH0=0.3705997      K1=0.4580187
+K2=2.151973E-3   K3=1E-3   K3B =1.885743   W0=1E-7   NLX =1.979533E-7
+DVT0W= 0   DVT1W= 0   DVT2W= 0   DVT0=0.4180247   DVT1=0.5426555
+DVT2=-0.5   U0=282.8516693   +UA=-1.479115E-9   UB=2.771868E-18
+UC=4.191212E-11   VSAT=1.567551E5   A0=1.7299219   AGS =0.3351874
+B0=-5.459641E-8   B1=2.281689E-6   KETA=-7.964814E-3   A1=1.404347E-4
+A2=0.3958259   RDSW=116.1842583   PRWG=0.5   PRWB=-0.2   WR=1
+WINT=0   LINT=5.662622E-9   XL=3E-8   XW=-4E-8   DWG =-3.48834E-9
+DWB =8.945939E-9   VOFF=-0.1026024   NFACTOR= 1.527547   CIT =0
+CDSC=2.4E-4   CDSCD= 0   CDSCB= 0   ETA0=5.273497E-3
```

+ETAB=6.155241E–4 DSUB=0.0328792 PCLM=1.8598332 PDIBLC1= 1
+PDIBLC2= 2.597071E–3 PDIBLCB= –0.0638656 DROUT= 0.8750173
+PSCBE1=3.733074E8 PSCBE2=3.1755E–8 PVAG=9.969483E–3 DELTA= 0.01
+RSH =4.5 MOBMOD=1 PRT =0 UTE =–1.5 KT1 =–0.11
+KT1L=0 KT2 =0.022 UA1 =4.31E–9 UB1 =–7.61E–18 UC1 =–5.6E–11
+AT=3.3E4 WL=0 WLN =1 WW=0 WWN =1 WWL =0
+LL=0 LLN =1 LW=0 LWN =1 LWL=0 CAPMOD=2
+XPART= 0.5 CGDO=3.8E–10 CGSO=3.8E–10 CGBO=1E–12 CJ=1.517652E–3
+PB=0.99 MJ=0.4042707 CJSW=4.19793E–10 PBSW=0.8315437
+MJSW=0.3795104 CJSWG=3.29E–10 PBSWG=0.8315437
+MJSWG=0.3795104 CF=0 PVTH0= –6.324971E–3 PRDSW= –10
+PK2=2.675691E–3 WKETA= –1.645688E–3 LKETA= –0.0122331)

BSIM3 SPICE MODEL FOR PMOS

.MODEL PMOS PMOS (
+VERSION= 3.1 LEVEL= 49 TNOM=27 TOX =5.6E–9 XJ=1E–7
+NCH =4.1589E17 VTH0=–0.5301873 K1=0.6176994 K2=–1.123056E–3 K3=0
+K3B =9.6084801 W0=1E–6 NLX =1E–9 DVT0W= 0 DVT1W= 0
+DVT2W= 0 DVT0=2.5278534 DVT1=0.7456063 DVT2=–0.1465105
+U0=104.8572245 UA=1.186639E–9 UB=1E–21 UC=–1E–10
+VSAT=1.909951E5 A0=0.8879722 AGS =0.1476076 B0=1.195257E–6
+B1=5E–6 KETA=0.0162687 A1=4.253866E–3 A2=0.3 RDSW=852.464666
+PRWG=0.2769343 PRWB=–0.2426706 WR=1 WINT=0 LINT=4.358485E–8
+XL=3E–8 XW=–4E–8 DWG =–2.561792E–8 DWB =3.107252E–9
+VOFF=–0.1240087 NFACTOR= 1.1688205 CIT =0 CDSC=2.4E–4
+CDSCD= 0 CDSCB= 0 ETA0=0.4082093 ETAB=–0.1429114
+DSUB=1.1220319 PCLM=1.2613618 PDIBLC1= 5.44991E–3
+PDIBLC2= –1.3578E–9 PDIBLCB= –1E–3 DROUT= 0.065719
+PSCBE1=1.157312E10 PSCBE2=1.046498E–9 PVAG=0.015388 DELTA= 0.01
+RSH =3.4 MOBMOD=1 PRT =0 UTE =–1.5 KT1 =–0.11
+KT1L=0 KT2 =0.022 UA1 =4.31E–9 UB1 =–7.61E–18 UC1 =–5.6E–11
+AT=3.3E4 WL=0 WLN =1 WW=0 WWN =1 WWL =0
+LL=0 LLN =1 LW=0 LWN =1 LWL =0 CAPMOD=2
+XPART= 0.5 CGDO=3.6E–10 CGSO=3.6E–10 CGBO=1E–12 CJ=1.88432E–3
+PB=0.99 MJ=0.4694628 CJSW=3.091997E–10 PBSW=0.7523248
+MJSW=0.2453993 CJSWG=2.5E–10 PBSWG=0.7523248 MJSWG=0.2453993
+CF=0 PVTH0= 3.936913E–3 PRDSW= 20.8071404 PK2 =2.437362E–3
+WKETA= 0.0196526 LKETA= –7.590931E–3)

Appendix B

MATLAB CODE

```
% MATLAB Program for Third Order Cascade ΣΔ Modulator

clear;
t0=clock;
bw=320 e3;                          % Base-band Bandwidth
R=64;                               % Oversampling Rate
Fs=R*2*bw;                          % Oversampling frequency
Ts=1/Fs;                            % Oversampling Period
N=65536;                            % Samples number
Fin=50 e3;                          % Input signal frequency
Ampl=0.3;                           % Input signal amplitude [V]
Ntransient=0

%
% kT/C noise and op-amp non-idealities
%

echo on;
k=1.38e-23;                         % Boltzmann Constant
Temp=300;                           % Absolute Temperature in Kelvin
Cf=5e-12;                           % Integrating Capacitance of the first integrator
Cp=3e-11;                           % Parasitic Capacitance
A=3160;                             % Op-amp Gain (70 dB Approx)
alpha=A*(Cf+Cp)/[A*(Cf+Cp)+(ai1*Cf)+(af1*Cf)];
                                    % A=Op-amp finite gain (alfa=(A-1)/A -> ideal
                                    op-amp alfa=1)
Amax=2.2;                           % Op-amp saturation value [V]
```

```
sr=20e6;                    % Op-amp slew rate [V/s]
GBW=200e6;                  % Op-amp GBW [Hz]
noise1=20e-6;               % 1st int. output noise std. dev.
[V/sqrt(Hz)]
delta=10e-9;                % Random Sampling jitter (std. dev.) [s] (Boser,
echo off;

% Modulator coefficients

echo on;
ai1=1.0;
af1=0.2;
ai2=0.5;
af2=0.25;
ai3=0.1;
au3=0.5;
af3=0.1;
Vref=1;
echo off;

finrad=Fin*2*pi;            % Input signal frequency in radians


s0=sprintf('** Simulation Parameters **');
s1=sprintf('  Fs(Hz)=%1.0f',Fs);
s2=sprintf('  Ts(s)=%1.6e',Ts);
s3=sprintf('  Fin(Hz)=%1.4f,Fin);
s4=sprintf('  BW(Hz)=%1.0f,bw);
s5=sprintf('  OSR=%1.0f,R);
s6=sprintf('  Npoints=%1.0f,N);
s7=sprintf('  tsim(sec)=%1.3f,N/Fs);
s8=sprintf('  Nperiods=%1.3f,N*Fin/Fs);
disp(s0)
disp(s1)
disp(s2)
disp(s3)
disp(s4)
disp(s5)
disp(s6)
disp(s7)
disp(s8)
```

```
% Open Simulink diagram first
options=simset('InitialState', zeros(1,6), 'RelTol', 1e-3, 'MaxStep', 1/Fs);
sim('SD3nonideal', (N+Ntransient)/Fs, options); % Starts Simulink simulation

%  Calculates SNR and PSD of the bit-stream and of the signal
w=hann(N);
echo on;
f=Fin/Fs                          % Normalized signal frequency
fB=N*(bw/Fs)                      % Base-band frequency bins
yy1=zeros(1,N);
yy1=yout(2+Ntransient:1+N+Ntransient)';
echo off;

ptot1=zeros(1,N);
[snr,ptot1]=calcSNR(yy1(1:N),f,fB,w,N,Vref);
Rbit=(snr-1.76)/6.02;             % Equivalent resolution in bits

% Output Graph
figure(1);
clf;
semilogx(linspace(0,Fs/2,N/2), ptot1(1:N/2), 'k');
grid on;
title('PSD of a 3rd-Order Sigma-Delta Modulator (Non-Ideal)')
xlabel('Frequency [Hz]')
ylabel('PSD [dB]')
axis([0 Fs/2 -200 0]);


%Hann Function%

function w = hann(n)
a0=0.338946;
a1=-0.481973;
a2=0.161054;
a3=-0.018027;
A=n*0.5*((a0*a0+0.5*(a1*a1+a2*a2+a3*a3))^0.5);
for i=1:n
w(i) = (a0+a1*cos(2*pi*(i-1)/n)+a2*cos(4*pi*(i-1)/n)+a3*cos(6*pi*(i-1)/n))/A;
end;
```

```
%
function y=dbp(x)
% dbp(x) = 10*log10(x): the dB equivalent of the power x
y = -Inf*ones(size(x));
nonzero = x~=0;
y(nonzero) = 10*log10(abs(x(nonzero)));
```

% Function for SNR

```
function [snrdB,ptotdB,psigdB,pnoisedB] = calcSNR(vout,f,fB,w,N,Vref)
% SNR calculation in the time domain
% vout: Sigma-Delta bit-stream taken at the modulator output
% f:   Normalized signal frequency (fs -> 1)
% fB:  Base-band frequency bins
% w:   windowing vector
% N:    samples number
% Vref: feedback reference voltage
%
% snrdB:      SNR in dB
% ptotdB:     Bit-stream power spectral density (vector)
% psigdB:     Extracted signal power spectral density (vector)
% pnoisedB:  Noise power spectral density (vector)
%
fB=ceil(fB);
signal=(N/sum(w))*sinusx(vout(1:N).*w,f,N);     % Extracts sinusoidal signal
noise=vout(1:N)-signal;                          % Extracts noise components
stot=((abs(fft((vout(1:N).*w)')))).^2);          % Bit-stream PSD
ssignal=(abs(fft((signal(1:N).*w)'))).^2;        % Signal PSD
snoise=(abs(fft((noise(1:N).*w)'))).^2;          % Noise PSD
pwsignal=sum(ssignal(1:fB));                     % Signal power
pwnoise=sum(snoise(1:fB));                       % Noise power
snr=pwsignal/pwnoise;
snrdB=dbp(snr);
norm=sum(stot)/Vref^2;                           % PSD normalization
if nargout > 1
        ptot=stot/norm;
        ptotdB=dbp(ptot);
end

if nargout > 2
```

```
        psig=ssignal/norm;
        psigdB=dbp(psig);
end

if nargout > 3
        pnoise=snoise/norm;
        pnoisedB=dbp(pnoise);
end;


%Function for Sinusoidal Extraction

function outx = sinusx(in,f,n)
%
sinx=sin(2*pi*f*[1:n]);
cosx=cos(2*pi*f*[1:n]);
in=in(1:n);
a1=2*sinx.*in;
a=sum(a1)/n;
b1=2*cosx.*in;
b=sum(b1)/n;
outx=a.*sinx + b.*cosx;

function out = slew(in,alfa,sr,GBW,Ts)
% Models the op-amp slew rate for a discrete time integrator
% in:  input signal amplitude
% alfa: effect of finite gain (ideal op-amp alfa=1)
% sr:  slew rate in V/s
% GBW: gain-bandwidth product of the integrator in Hz
% Ts:  sample time
% out: output signal amplitude

tau=1/(2*pi*GBW);  % Time constant of the integrator
Tmax = Ts/2;

slope=alfa*abs(in)/tau;

if slope > sr                    % Op-amp in slewing
        tsl = abs(in)*alfa/sr - tau;  % Slewing time
        if tsl >= Tmax
                error = abs(in) - sr*Tmax;
```

```
        else
                texp = Tmax - tsl;
                error = abs(in)*(1-alfa) + (alfa*abs(in) - sr*tsl) * exp(-texp/tau);
        end
else                                    % Op-amp in linear region
        texp = Tmax;
        error = abs(in)*(1-alfa) + alfa*abs(in) * exp(-texp/tau);
end
out = in - sign(in)*error;
```

Appendix C

SNR CALCULATION

The SNR of a modulator is defined as

$$SNR = \frac{P_S}{P_N} \tag{C.1}$$

where P_S denotes the signal power and P_N the noise power. In an ideal ΣΔ modulator, the SNR is determined only by the quantization noise according to

$$SNR = \frac{\frac{\Delta^2}{8}}{P_N} = \frac{2^{2N}3(2L+1)M^{2L+1}}{2\pi^{2L}} \tag{C.2}$$

where Δ denotes the input range of the ΣΔ modulator, N the number of bits in the quantizer, M the oversampling ratio, and L the order of the ΣΔ modulator.

However, the other noise or distortion sources increase the total noise power of the data converter above the quantization noise level and contribute to the SNR [12].

The calculation of the SNR of a ΣΔ modulator starting from the raw output data (output samples) is performed in two steps. In the first step, the sinusoidal signal (S) is extracted from the sequence of N_O output data (O_i, at time t_i), typically by computing a discrete Fourier transform (DFT) of O at the signal frequency (f_{in})

$$\begin{aligned} S(t_j) = &\frac{1}{N_O}\left(\sum_{i=1}^{N_O} 2O_iW_i\cos(2\pi f_{in}t_i)\right)\cos(2\pi f_{in}t_j) \\ &+\frac{1}{N_O}\left(\sum_{i=1}^{N_O} 2O_iW_i\sin(2\pi f_{in}t_i)\right)\sin(2\pi f_{in}t_j) \end{aligned} \tag{C.3}$$

where W_i denotes the desired window for the data. The obtained signal is then subtracted from the raw output signal in the time domain, thus obtaining a signal (N_T) which contains only the noise and distortion contributions. In the second step, we calculate the FFT of S and of N_T, obtaining the spectra of the signal (S_S) and of the noise (S_N) . The same window W_i used for the DFT has to be used also for the FFT. Finally, the signal (P_S) and noise power (P_N) are calculated by integrating the power spectra

$$P_S = \sum_{i=1}^{N_B} S_S^{\,2}(i) \quad and \quad P_N = \sum_{i=1}^{N_B} S_N^{\,2}(i) \tag{C.4}$$

where $N_B=(N_O BW)/f_S$, denotes the number of samples corresponding to the desired BW (baseband, BW) with sampling frequency f_S. The SNR is then obtained from (C.1).

The spectra in Figures 5.2, 5.6 and 5.13 were estimated by computing 64K point discrete Fourier transform of a windowed version of the output. The particular window (W_i) used was defined as follows:

$$w[n] = \frac{1}{A}\sum_{k=0}^{3} a_K \cos(2\pi kn/N), \qquad 0 \le n < N \tag{C.5}$$

where,

$$\begin{aligned} N &= 65536 \\ a_0 &= 0.338946 \\ a_1 &= -0.481973 \\ a_2 &= 0.161054 \\ a_3 &= -0.018027 \end{aligned} \tag{C.6}$$

$$A = \frac{N\Delta}{4}\sqrt{a_0^{\,2} + \frac{1}{2}\left(a_1^{\,2} + a_2^{\,2} + a_3^{\,2}\right)} \tag{C.7}$$

The scaling factor, A, is defined such that when a sinusoid with a peak–to–peak amplitude of Δ is windowed and the discrete Fourier transform is computed, the resulting spectral power will be unity, or 0 dB.